T10/00-408r0

Discussion of Eye Mask Proposal for Ultra320 SCSI with AAF (T10/00-400r0)

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Introduction

- Purpose of T10/00-400r0:
  - Define the input signal requirements for Ultra320 SCSI receivers using AAF compensation,
  - Set minimum requirements for that compensation,
  - Allow evaluation of input signal quality in applications without detailed knowledge of the particular AAF compensation circuitry.
- Purpose of this presentation:
  - Discuss the details of the T10/00-400r0 proposal,
  - Show how the proposed signal requirements fit to measured data for a few example configurations.

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Outline of Proposed AAF Signal Requirements

- AAF compensates for frequency-dependent attenuation by boosting the high frequency components of the signal.
- Eye masks establish the minimum AC amplitudes for free-running clock patterns and for all transitions including isolated pulses (i.e., a standard eye diagram).
- Eye masks include allowances for attenuation, crosstalk, and reflections.
- Any DC component of the input differential signal is removed before testing the AC waveform against the eye mask limits.
- Low frequency input signal characteristics are defined separately by specifying low frequency amplitude range and maximum differential DC component.
- Basic signal patterns to be tested are in the training pattern for paced transfers in SPI-4.
- Measured system waveforms can be tested against the proposed limits and eye masks by straight-forward manipulation of waveform files captured with a digital sampling oscilloscope.

Low Frequency Input Signal Requirements

- Low Freq amplitude: 600 mV < $|V_A| + |V_N|$ < 1.7 V pk-pk
- DC component: -50 mV < $[(|V_A| - |V_N|) / 2]$ < 50 mV
- These numbers are derived directly from SPI-4 requirements for driver amplitude and symmetry, and terminator tolerances with added allowances for cable and back-plane resistance.

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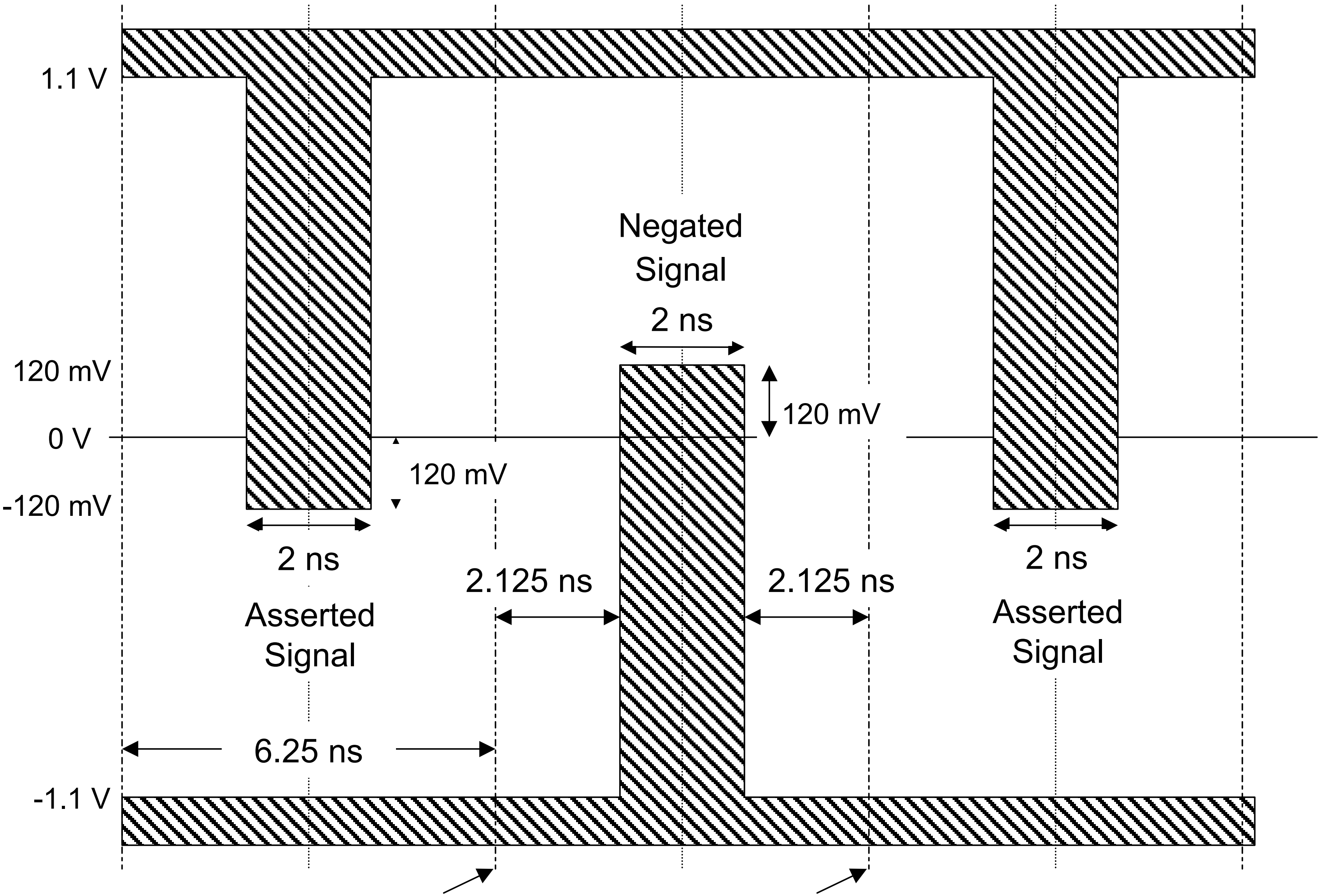
AC Input Signal Requirements

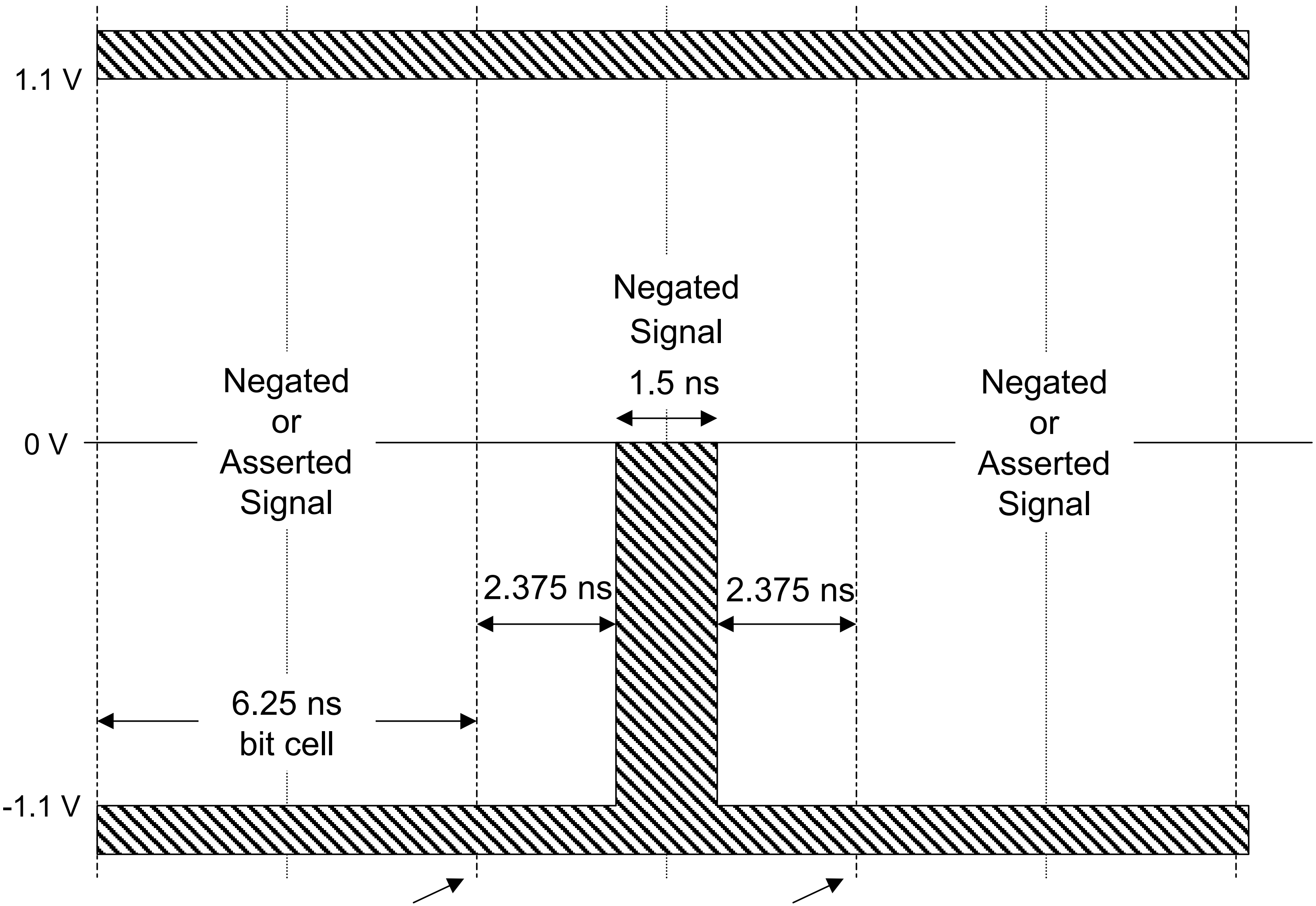
- With the DC component of the input signal removed:
  - The free-running clock and settled 1010 patterns shall exceed 120 mV peak for 2 ns centered on the bit-cell center.
    - For a sine-like waveform, this corresponds to a peak 1010 pattern that is 45% of the 300 mV minimum peak low frequency amplitude.
  - For random data, including isolated pulses:
    - Negated signals shall exceed 0 volts for a 1.5 ns interval, centered on the bit cell center as defined by the free-running clock de-skew pattern.
    - Asserted signals shall remain less than 0 volts for a 1.5 ns interval, centered on the bit-cell center as defined by the free-running clock de-skew pattern.
    - These requirements correspond to a “just open” eye.
- The following eye masks allow testing system waveforms against these AC requirements:

AAF Receiver Mask for settled 1010



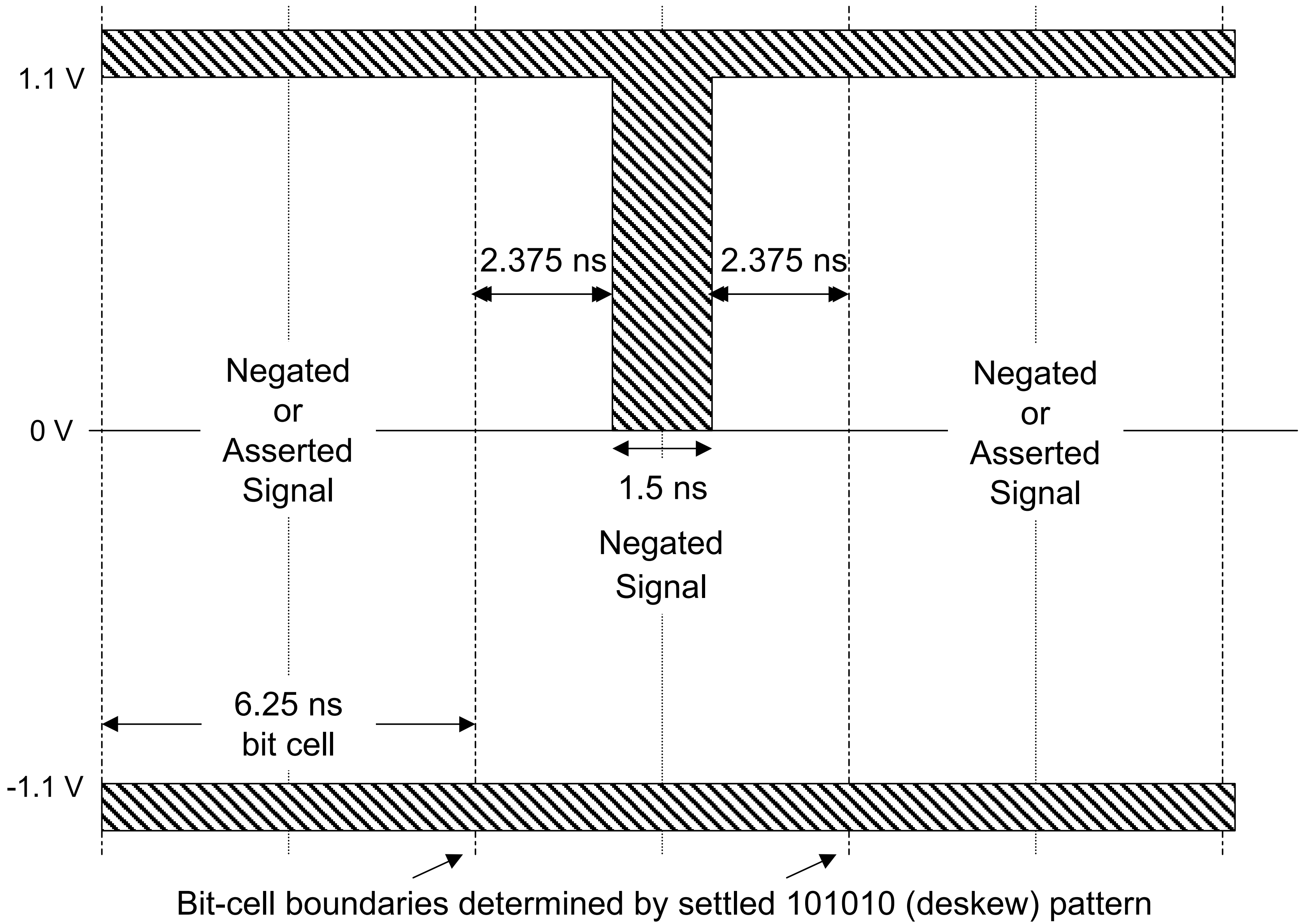
Bit-cell boundaries determined by settled 101010 pattern

AAF Receiver Mask for X-0-X patterns



Bit-cell boundaries determined by settled 101010 pattern

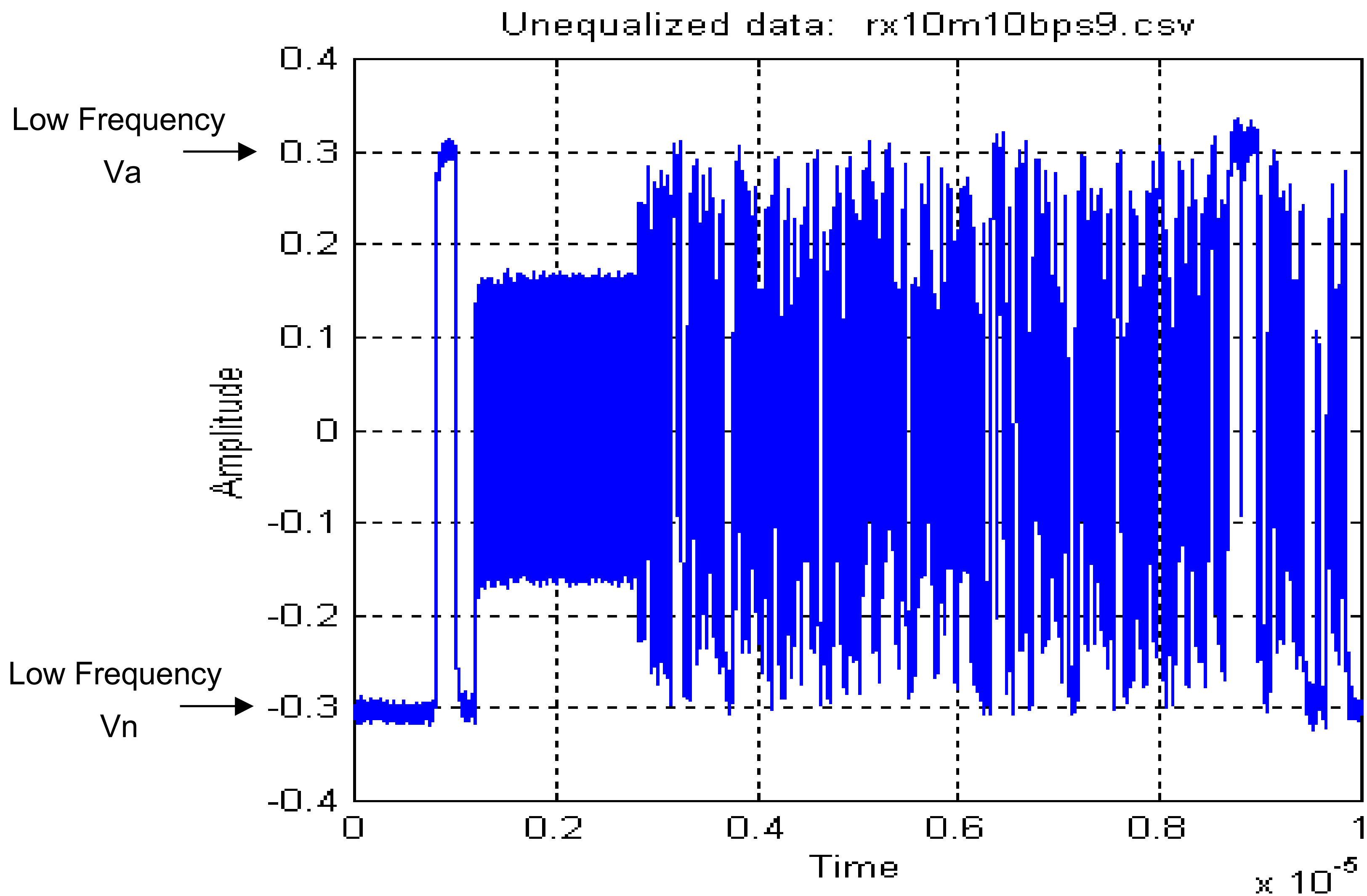
AAF Receiver Mask for X-1-X patterns



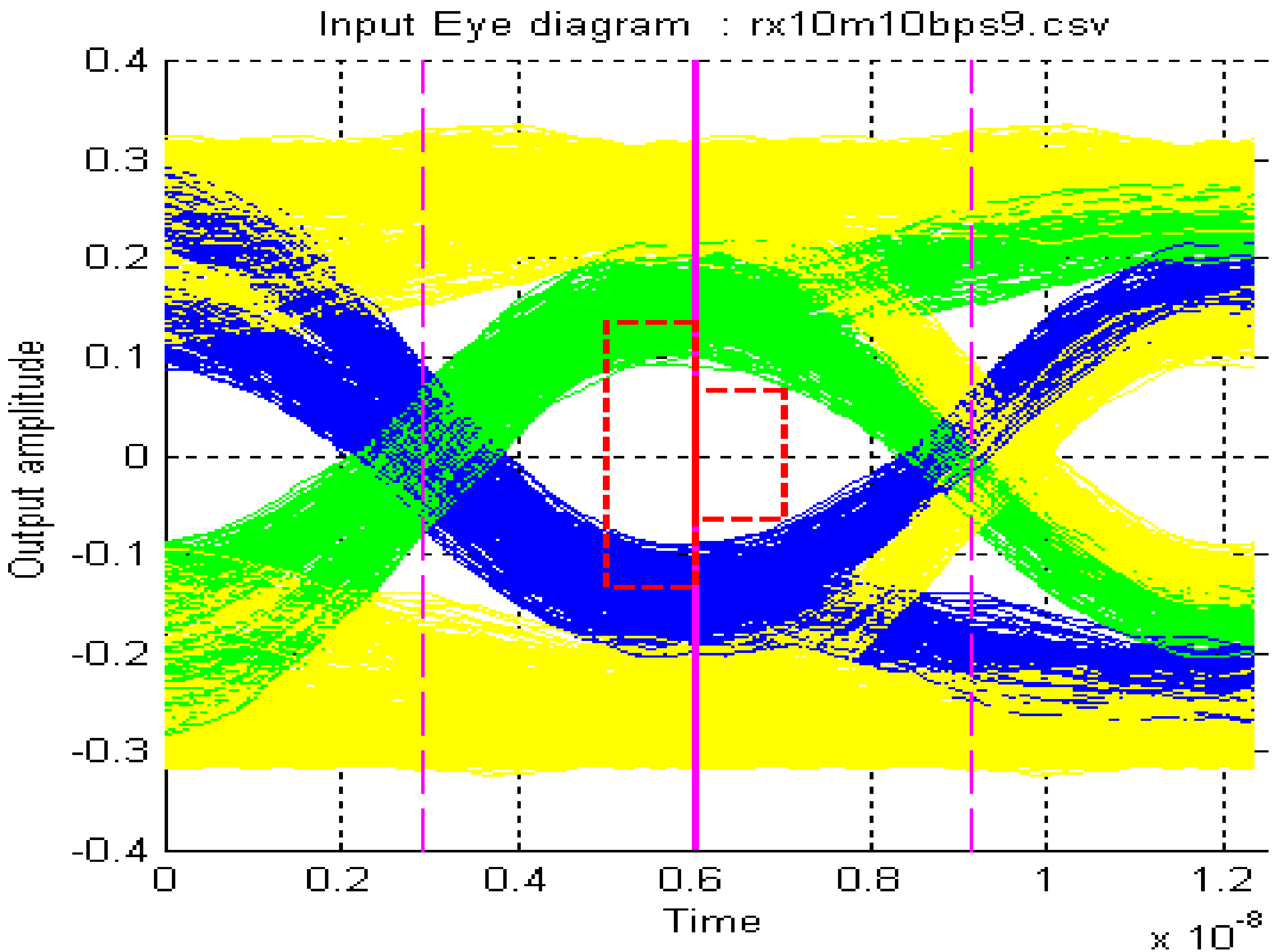
Examples

- The following slides show sample waveforms captured on 3 different cable configurations, with the minimum 600 mV peak-to-peak low frequency amplitude at the receiver.
- Configurations are 10-meter round, and 10-meter, and 0.7-meter twisted-flat cables to a 10-slot backplane.
- Diagrams for each configuration are:
  - Un-equalized input signal waveform,
  - Input eye diagram, with ±135 mV by ±1 ns mask representing total final amplitude and timing errors as in our previous presentations (this is updated from 150 mV that we used previously to reflect the new SPI-4 driver symmetry numbers),
  - 1010 input pattern on the proposed 1010 mask,
  - x1x patterns on the proposed x1x mask (x0x pattern results are similar),
  - Equalized eye diagram, with ±135 mV by ±1 ns mask representing total final amplitude and timing errors.

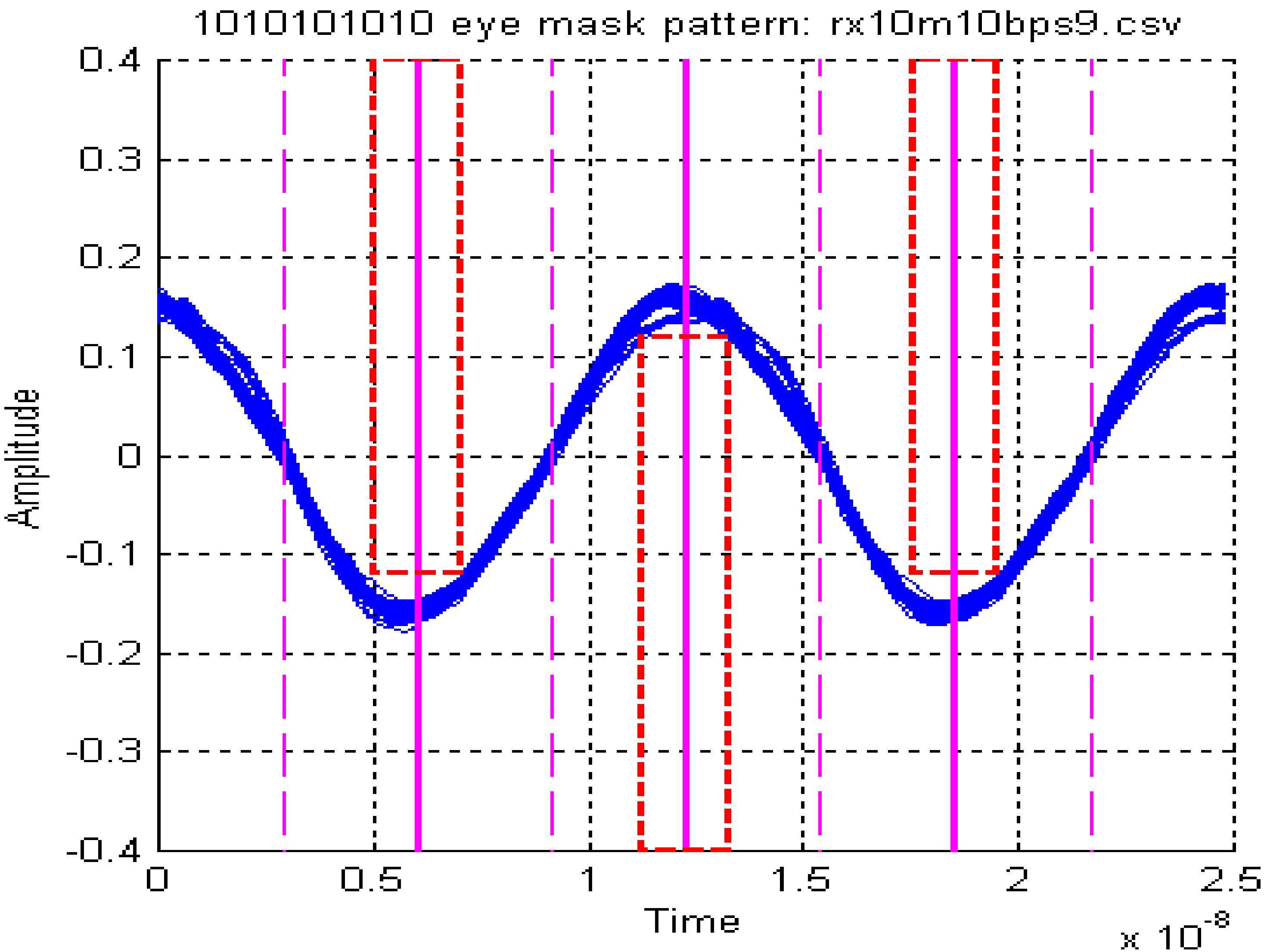
10m Round to 10-slot BP, 300 mV pk



10m Round to 10-slot BP, 300 mV pk



10m Round to 10-slot BP, 300 mV pk



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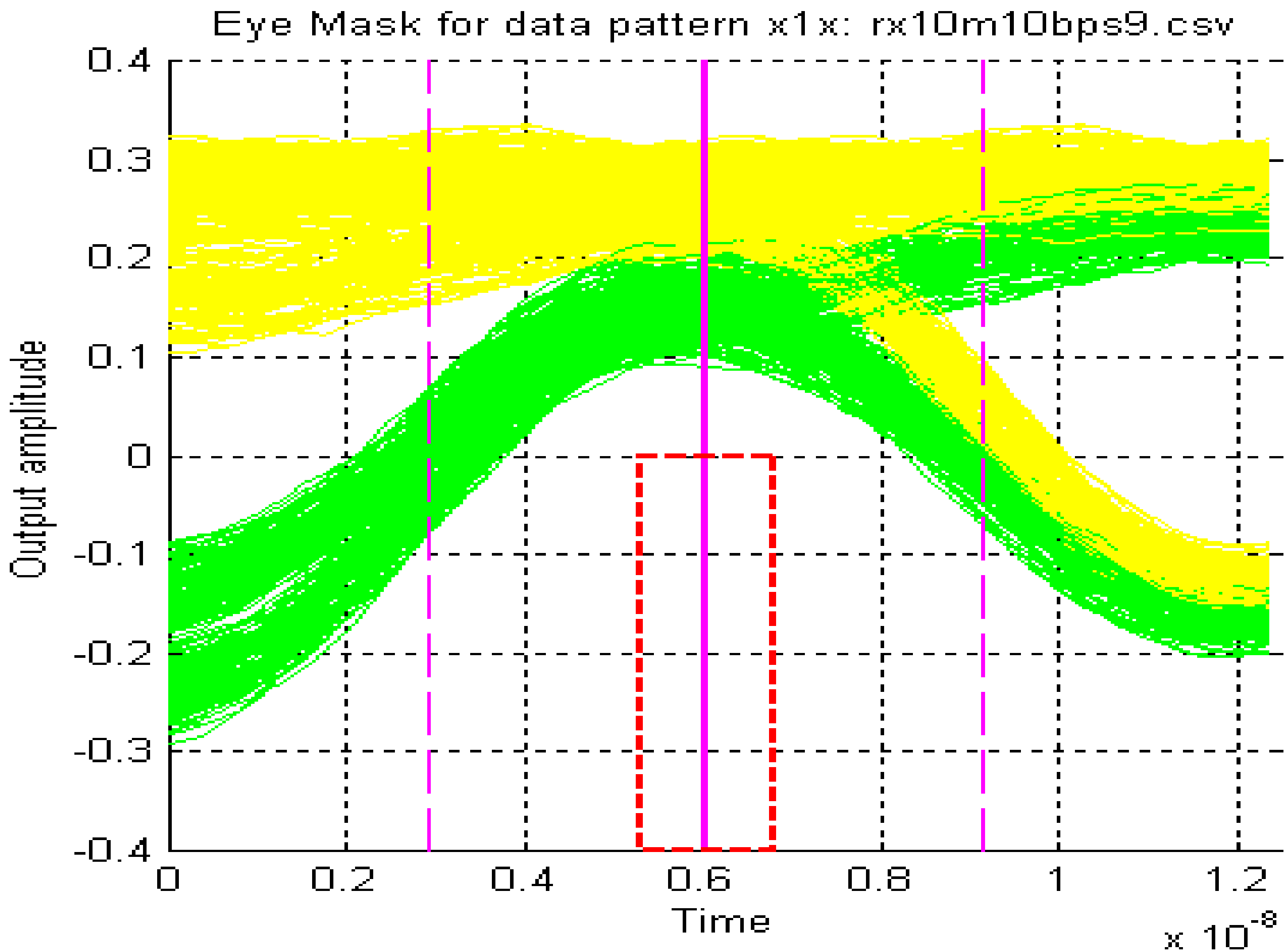
10m Round to 10-slot BP, 300 mV pk



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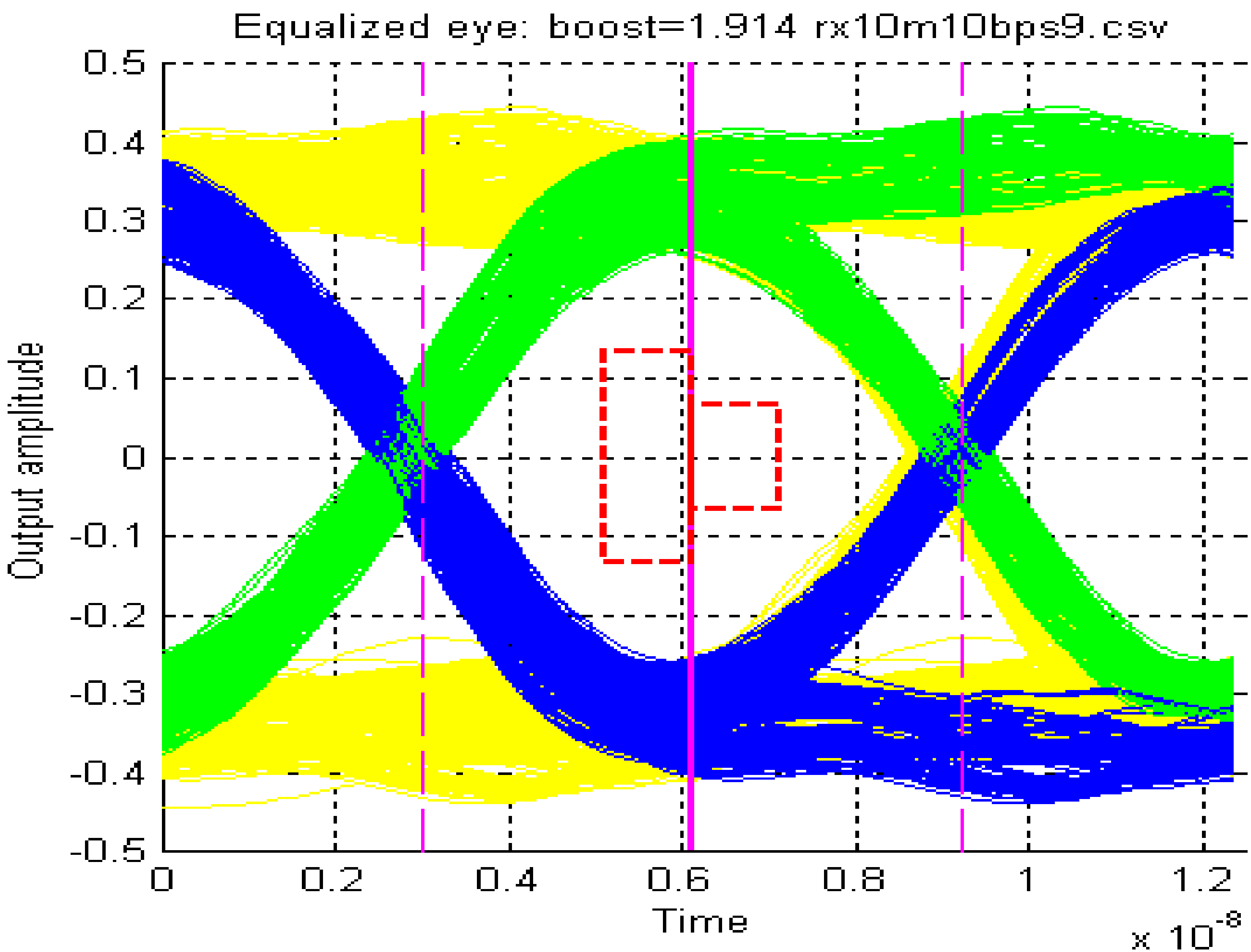
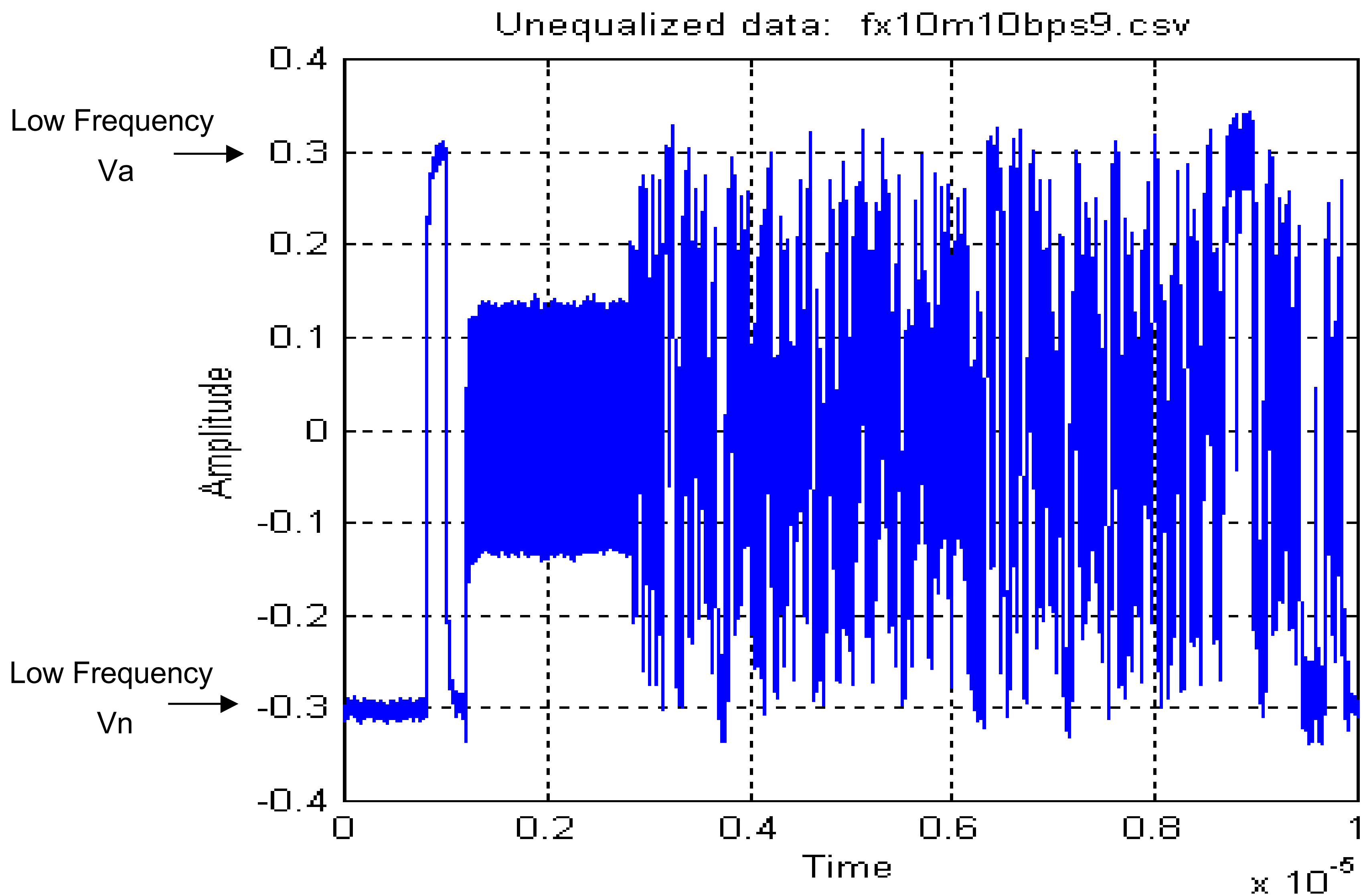
10m Round to 10-slot BP, 300 mV pk



10m Twisted-Flat to 10-slot BP, 300 mV pk



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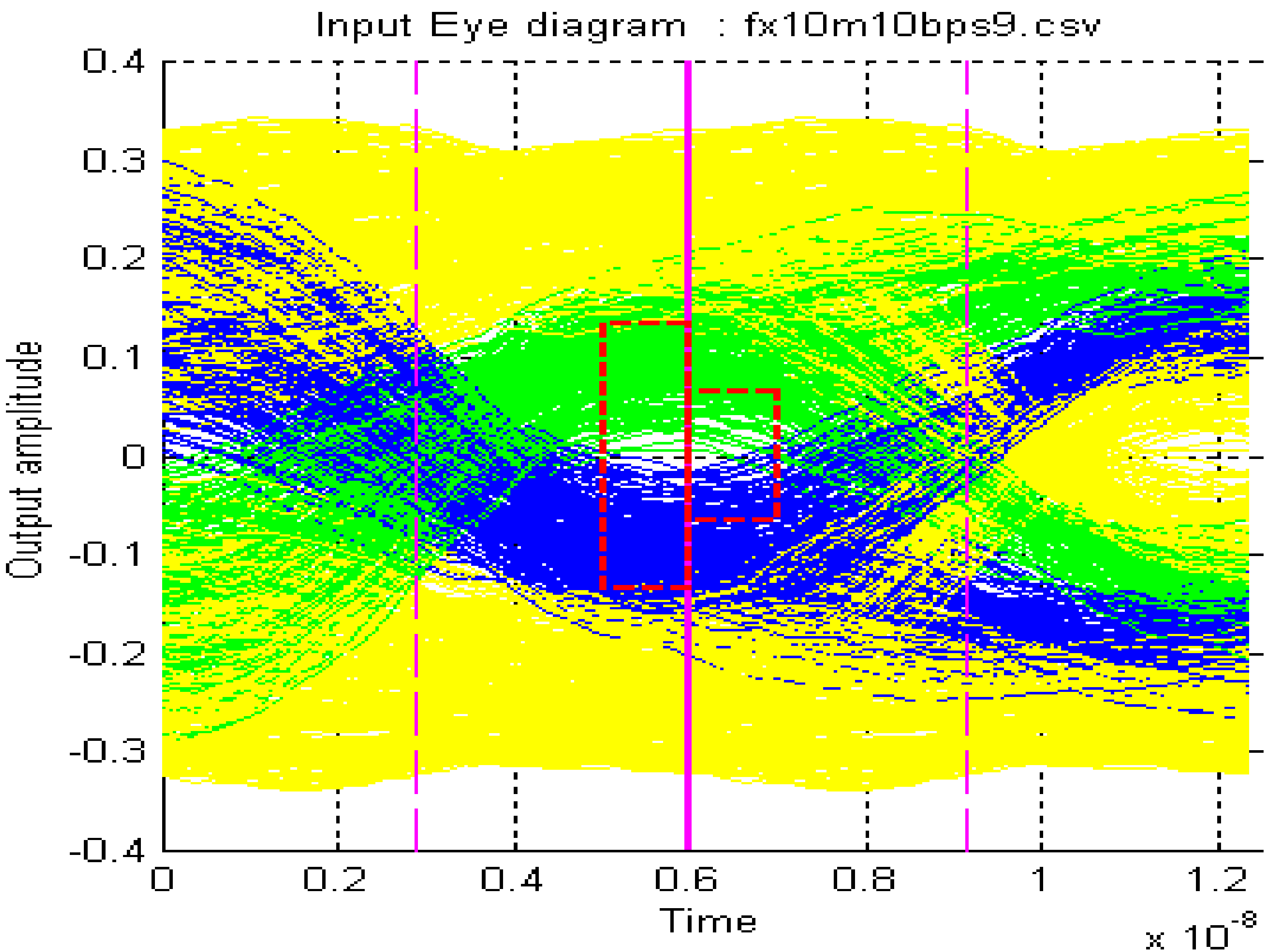
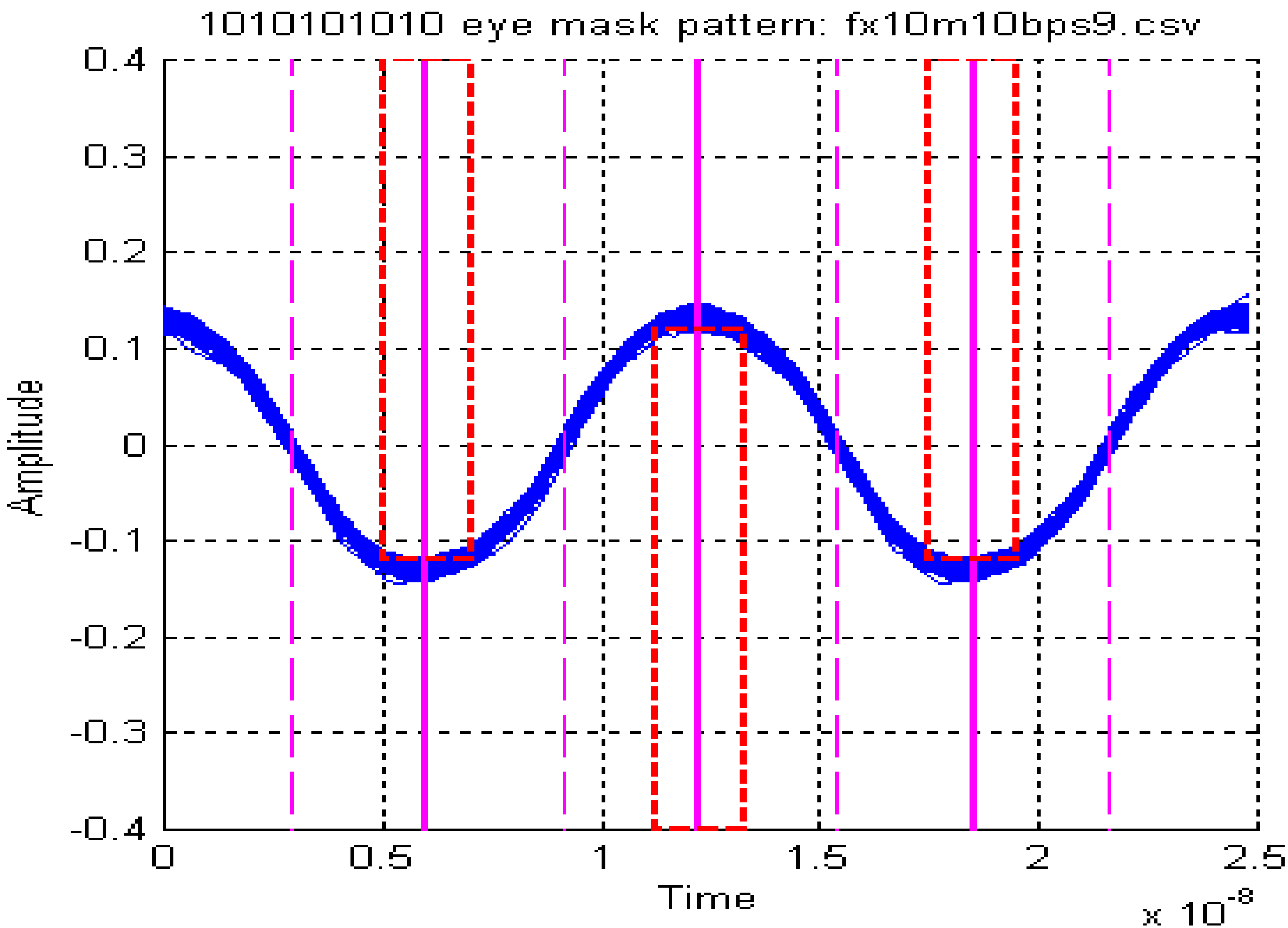
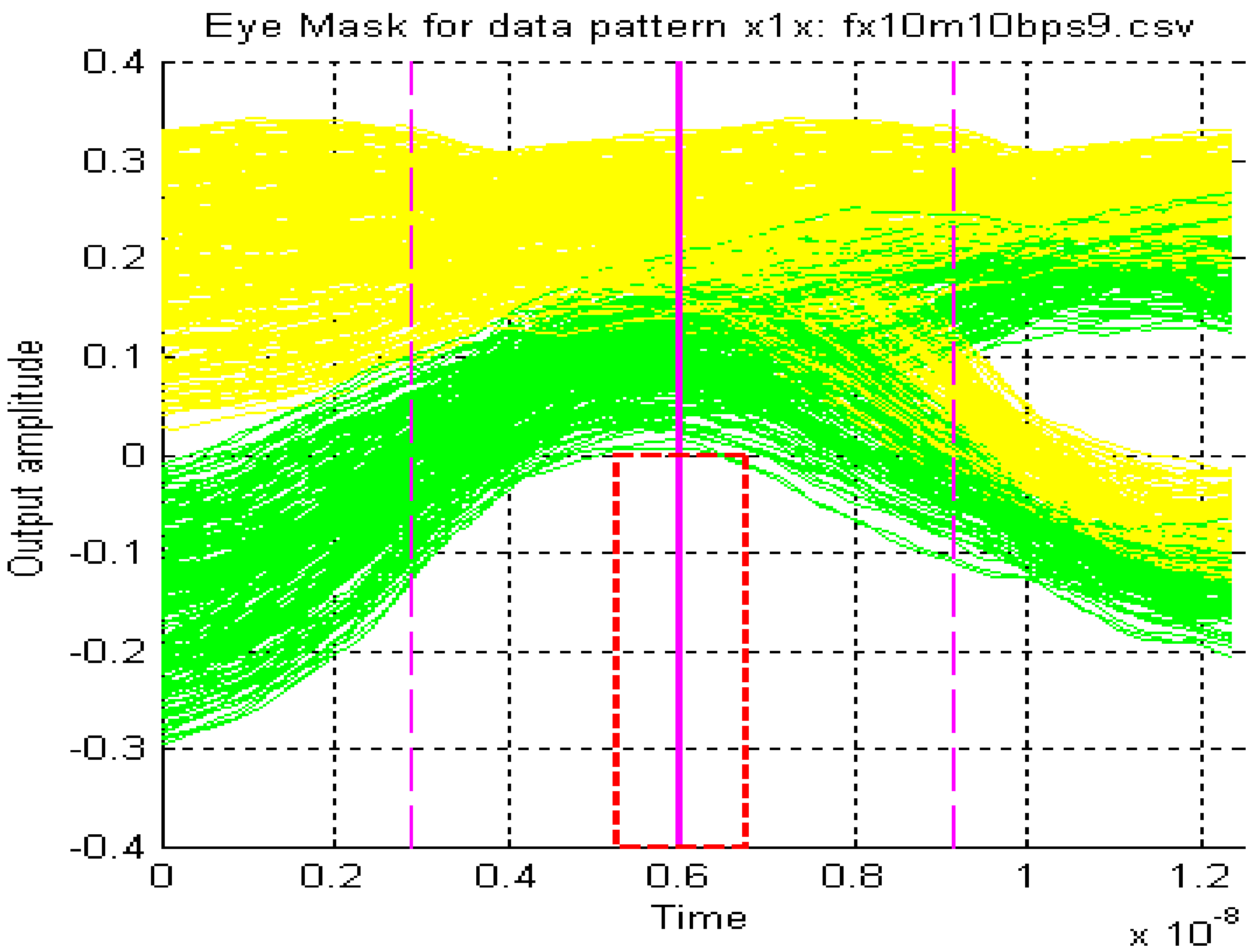
10m Twisted-Flat to 10-slot BP, 300 mV pk



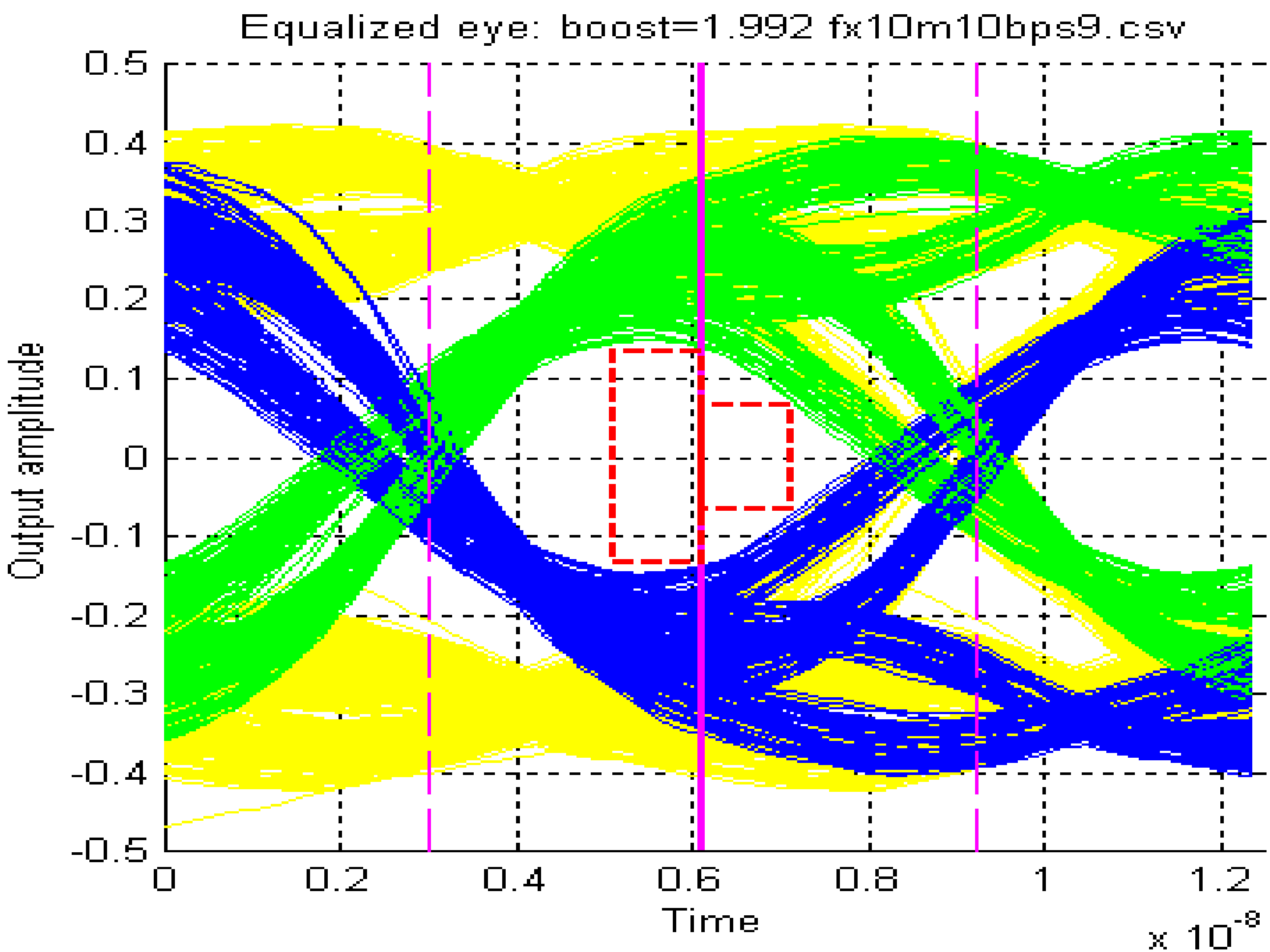
Quantum™ 10m Twisted-Flat to 10-slot BP, 300 mV pk



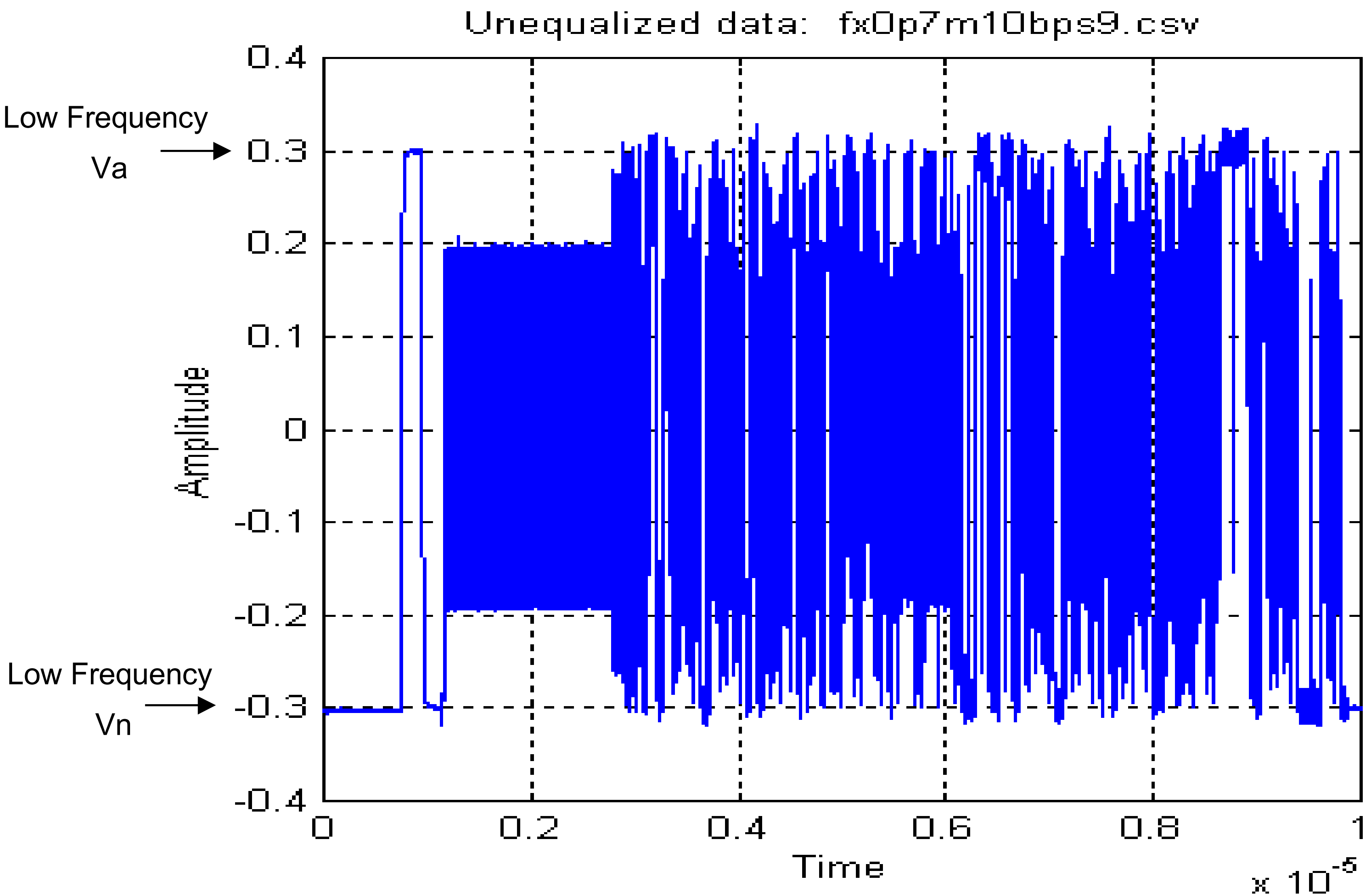
10m Twisted-Flat to 10-slot BP, 300 mV pk



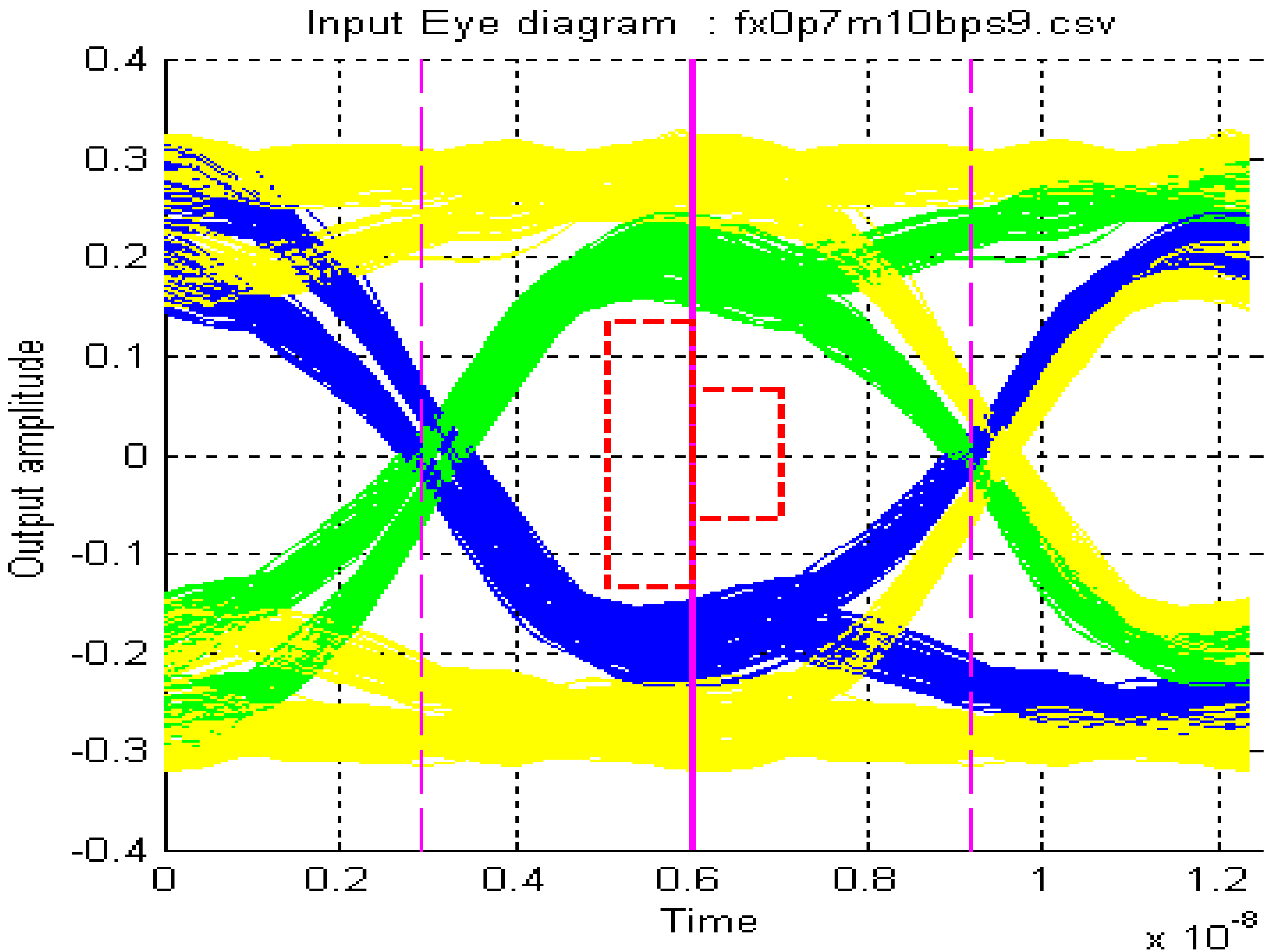
10m Twisted-Flat to 10-slot BP, 300 mV pk



0.7m Tw-Flat to 10-slot BP, 300 mV pk



0.7m Tw-Flat to 10-slot BP, 300 mV pk



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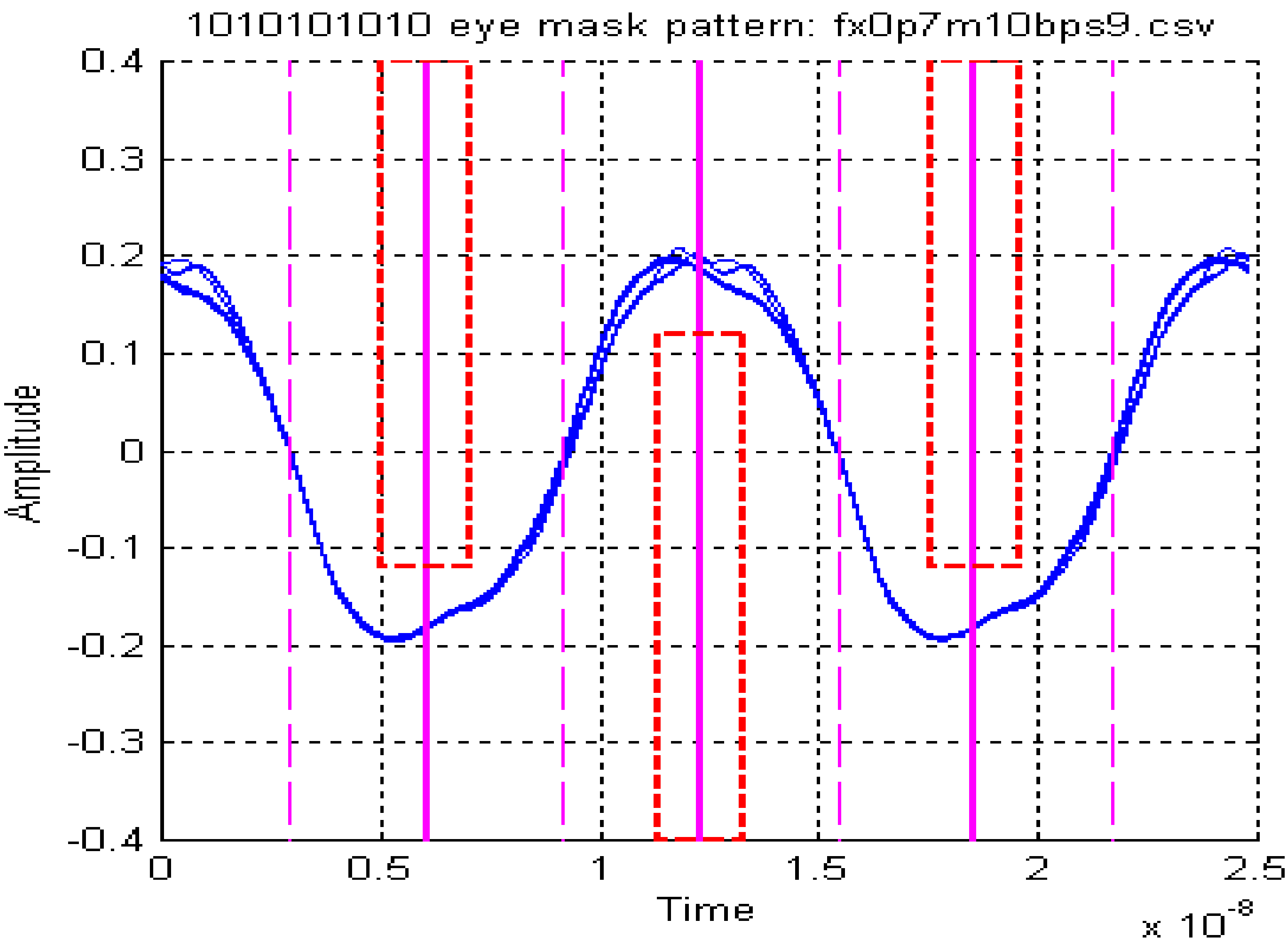
0.7m Tw-Flat to 10-slot BP, 300 mV pk



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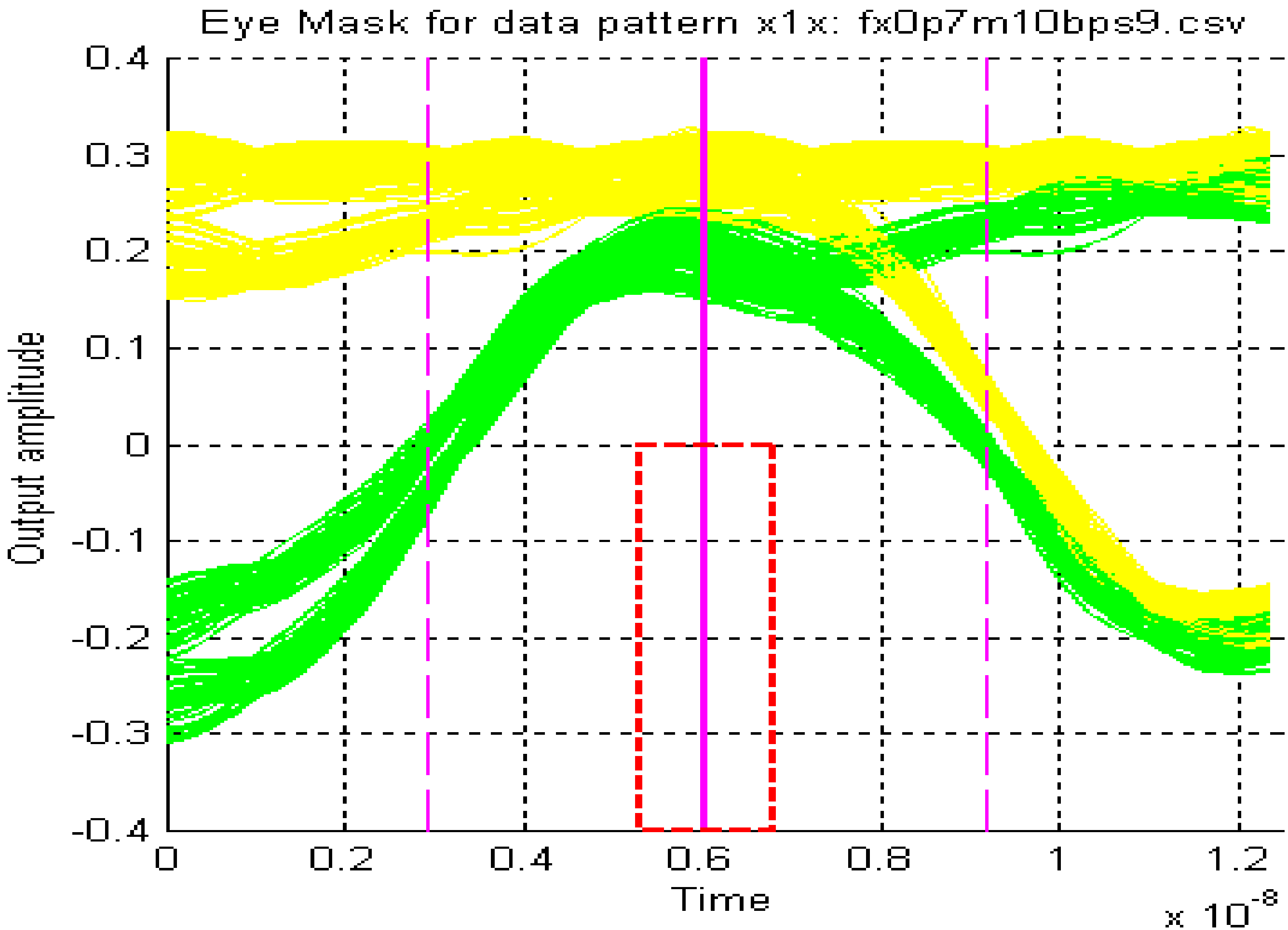
0.7m Tw-Flat to 10-slot BP, 300 mV pk



0.7m Tw-Flat to 10-slot BP, 300 mV pk