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To: **T10 Technical committee**
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Subject: Proposal for Ultra320 AAF receiver input signal specification for SPI-4

Introduction

The following is a proposal defining the input signal requirements for Ultra320 SCSI receivers using AAF compensation, and thus sets the minimum requirements for that compensation. This proposal also allows evaluation of the input signal quality in an application without requiring detailed knowledge of the particular AAF compensation circuitry in the receiver.

The AAF function compensates for frequency-dependent transmission path attenuation by boosting the high frequency components of the received signal. Masks are included to establish the minimum AC amplitudes for free-running clock and settled maximum frequency ("1010") patterns, the minimum amplitude of bit transitions, and the minimum eye diagram opening for all transitions. Two additional masks are split to treat x-1-x (don't care – assertion – don't care) and x-0-x (don't care – negation – don't care) data patterns separately to permit easier testing of an almost-closed eye pattern. These masks are used to establish AC signal amplitudes. Any DC offset component of the input signal must be removed before applying the overall eye diagram mask.

The low frequency receiver characteristics are defined by separately specifying a low frequency signal amplitude range and maximum DC offset component of the receiver input waveform. These low frequency requirements are derived directly from the specifications listed elsewhere in SPI-4 for driver amplitude range and symmetry, terminator tolerances and cable resistance, with an added allowance of 12 ohms maximum for back-plane resistance. The resulting numbers are included in this receiver input signal specification for clarity.

All references in the following are to the draft standard SCSI Parallel Interface – 4 (SPI-4) revision 3. That document is available at ftp://ftp.t10.org/t10/drafts/spi4/spi4r03.pdf.

The following are input signal requirements for a receiver incorporating AAF. These are for individual signals only:

For receivers incorporating AAF compensation, the input signal waveforms shall meet all of the following five amplitude and timing requirements.

1. Low frequency signal amplitude:

   The differential low frequency signal amplitude at the receiver during normal data shall fall within the following limits:

   600 mV < |Va| + |Vn| < 1.7 V peak-to-peak,

   The low frequency signal amplitudes shall be measured after 100 ns continuous assertion (or negation), and may be measured in the training pattern defined in clause 10.8.4.2.

2. Differential Offset:

   The differential offset component of the receiver input waveform, defined as the mid-point of the low frequency asserted and negated levels, shall be less than 50 mV.

   -50 mV < [(|Va| - |Vn|) ÷ 2] < 50 mV

   The low frequency signal amplitudes shall be measured after 100 ns continuous assertion (or negation), and may be measured in the training pattern defined in clause 10.8.4.2.

3. Free-running clock and settled 1010 pattern amplitude (a settled 1010 pattern is a 1010 pattern preceded by a minimum of 10 bit-cells of 1010 pattern):

   The free-running clock and settled 1010 data pattern amplitude, VCLKPP, is defined as the sum of the minimum negated and asserted amplitudes, each measured within a 2 ns interval centered on the appropriate bit-cell centers as shown in Figure 1. The bit-cell boundaries are defined as the average zero crossings of a settled 1010 pattern. The bit-cell center is the mid-point between bit-cell boundaries. The measured data waveform shall be band-limited to 200 MHz.

   VCLKPP > 240 mV

4. All-transition amplitude requirement:

   The amplitude change at all transitions shall exceed 100 mV measured as shown Figure 2. The measured data waveform shall be band-limited to 200 MHz.

5. Receiver Input Eye Masks

   a) Eye diagram mask: The eye diagram formed by superimposing the waveforms of all bit cells of the input data pattern shall be open for 1.5 ns centered on bit-cell center as shown in Figure 3, where bit-cell center is determined by the location of a settled 1010 clock pattern in the input waveform.

   b) All-transitions x-0-x (don't care – negation – don't care) and x-1-x (don't care – assertion – don't care) masks: Figure 4 and Figure 5, when combined, form the traditional eye mask shown in Figure 3 with limits that permit the eye to be nearly closed. For a negated signal, the receiver input waveform shall exceed 5 mV for 1.5 ns centered on the bit-cell center as defined by the free-running clock pattern (see Figure 4). For an asserted signal, the receiver input waveform shall remain less than -5 mV for 1.5 ns centered on the bit-cell center (see Figure 5).

The receiver input masks are concerned with the “AC” components of the input waveform only, and any DC term as calculated in requirement 2 above shall be removed before applying the test mask. The measured data waveform shall be band-limited to 200 MHz.

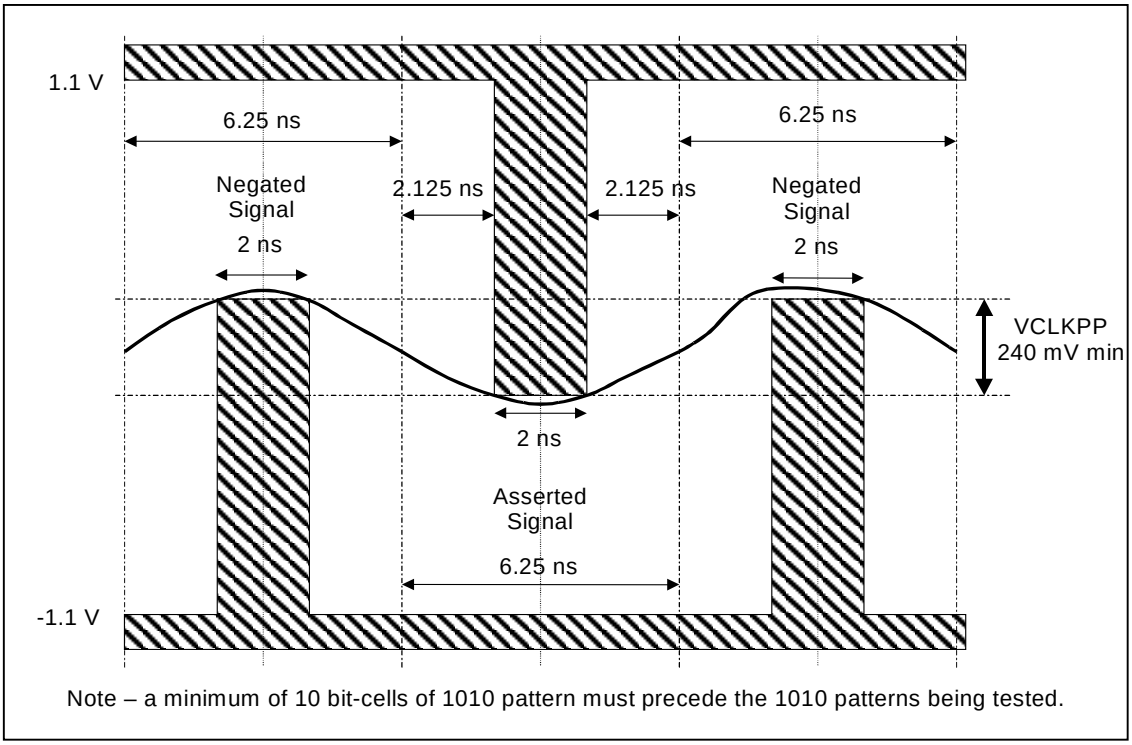

Figure 1 – Fast-160 AAF receiver mask showing VCLKPP on a free-running clock with a settled 1010 pattern

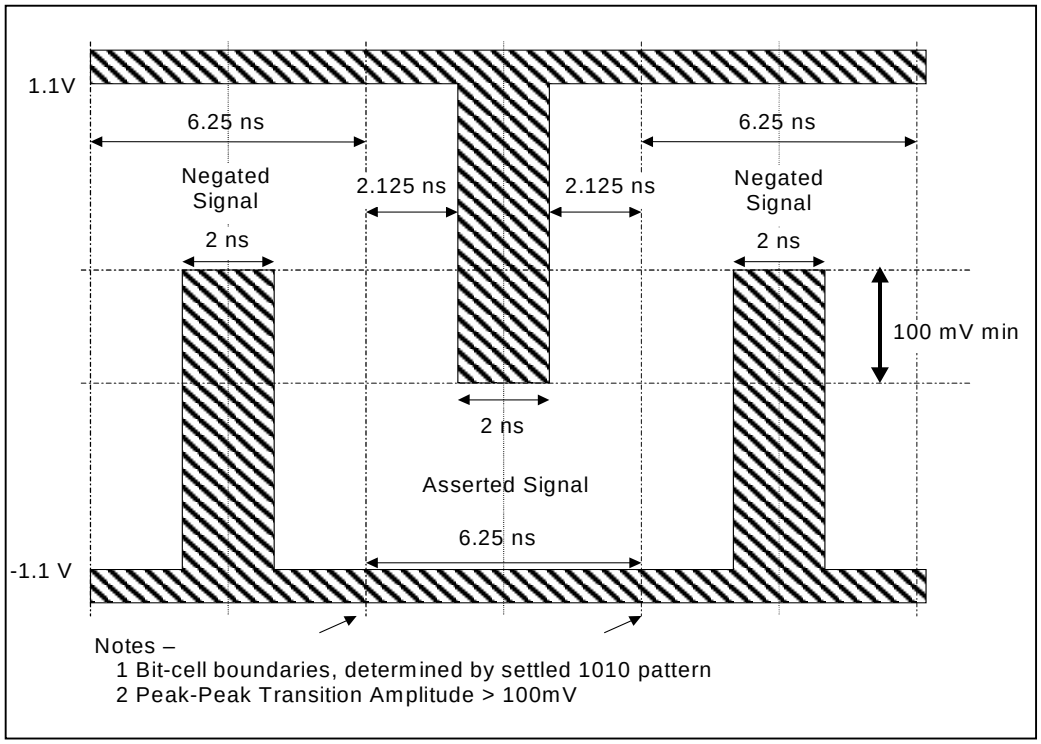

Figure 2 – Fast-160 AAF receiver mask showing minimum amplitude change for all signals

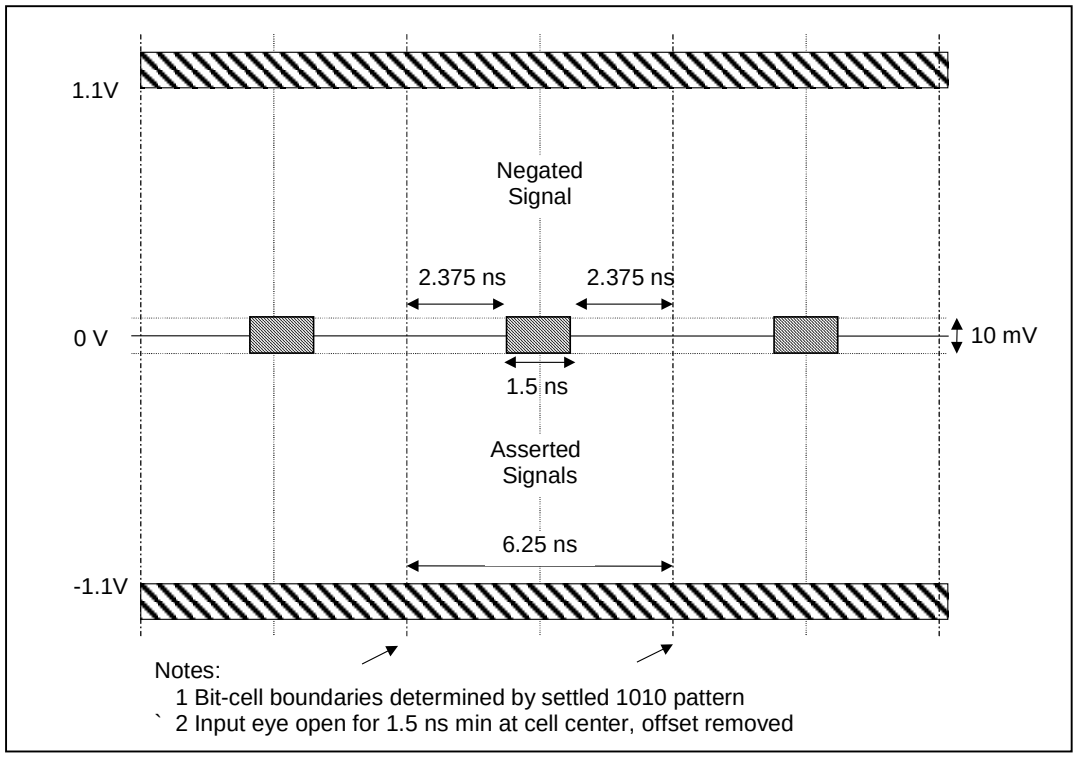

Figure 3 – Fast-160 receiver mask eye diagram, offset removed

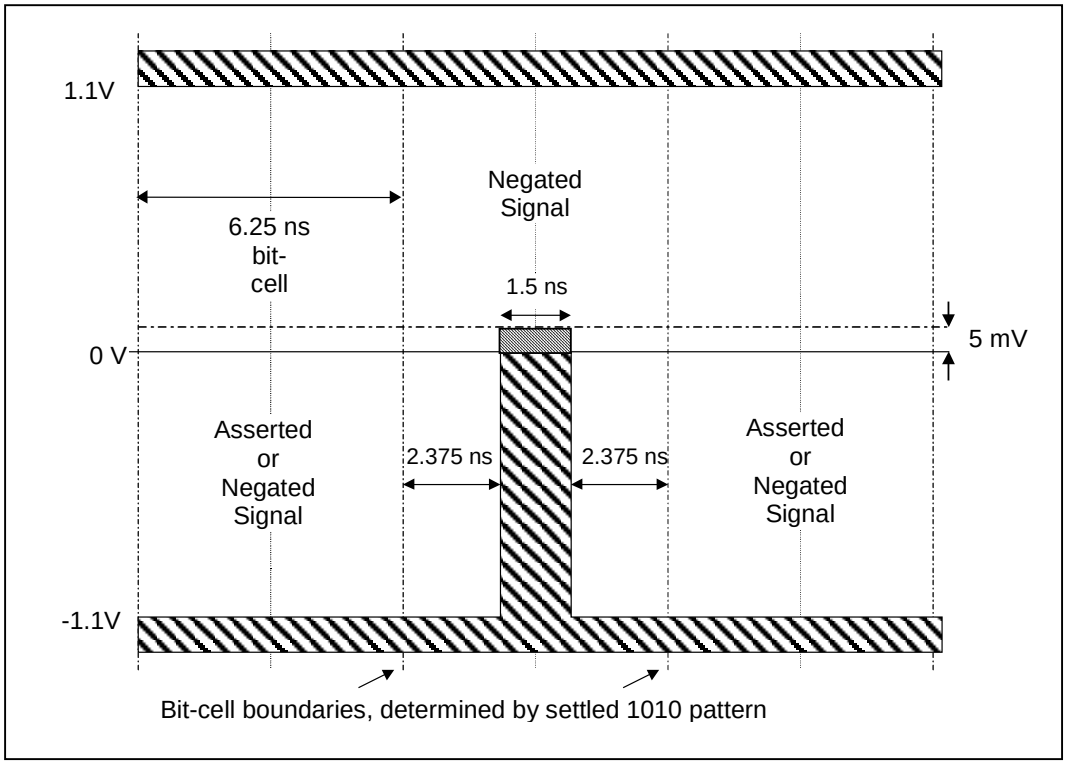

Figure 4 – Fast-160 AAF Receiver Mask for x-0-x patterns, offset removed

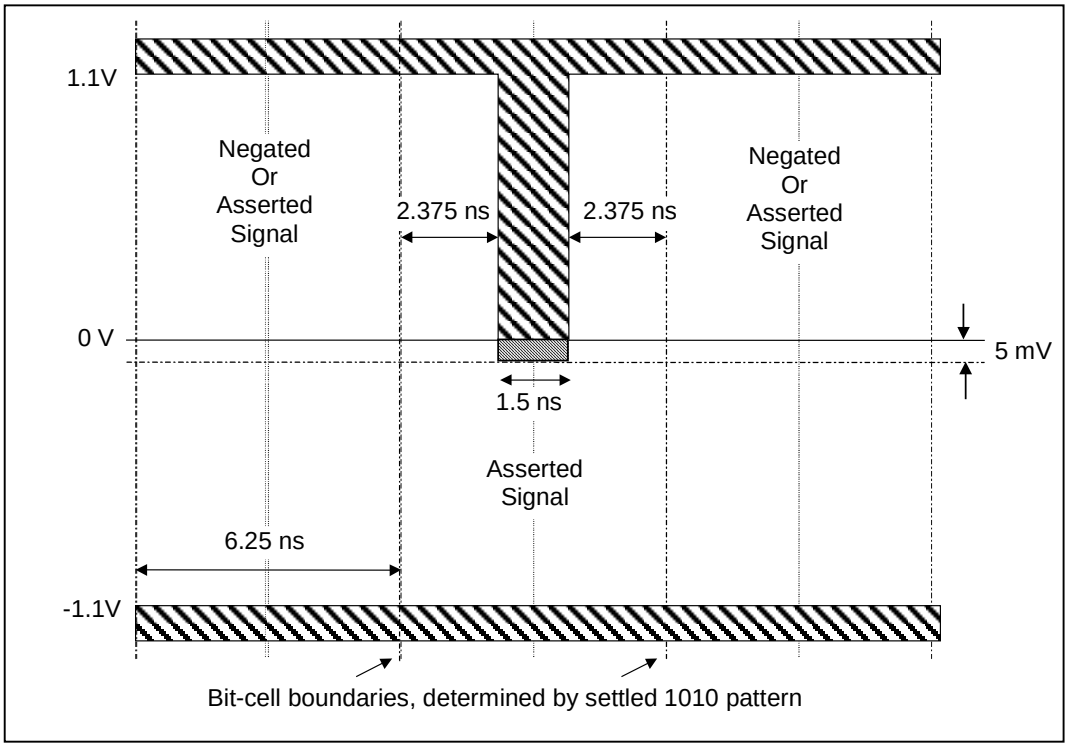

Figure 5 – Fast-160 AAF Receiver Mask for 1-0-1 patterns, offset removed