

Quantum™

Quantum Corporation
500 McCarthy Boulevard
Milpitas, CA 95035 USA

To: T10 Technical committee
From: Russ Brown
Phone: 613-599-2804
Email: russ.brown@quantum.com
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Subject: Proposal for Ultra320 AAF receiver input signal specification for SPI-4

Introduction

The following is a proposal defining the input signal requirements for Ultra320 SCSI receivers using AAF compensation, and thus sets the minimum requirements for that compensation. This proposal also allows evaluation of the input signal quality in an application without requiring detailed knowledge of the particular AAF compensation circuitry in the receiver.

The AAF function compensates for frequency-dependent transmission path attenuation by boosting the high frequency components of the received signal. Eye masks are included to establish the minimum AC amplitudes for free-running clock and settled maximum frequency ("101010") patterns (see Mask1), and for all transitions including isolated pulses (Mask 2a plus Mask 2b). Since these eye masks are used to establish AC signal amplitudes, any DC offset component of the input signal must be removed before applying the masks.

The low frequency receiver characteristics are defined by separately specifying a low frequency signal amplitude range and maximum DC offset component of the receiver input waveform. These low frequency requirements are derived directly from the specifications listed elsewhere in SPI-4 for Driver amplitude range and symmetry, terminator tolerances and cable resistance, with an added allowance of 12 ohms max for back-plane resistance. The resulting numbers are included in this receiver input signal specification for clarity.

Mask 2a and Mask 2b together define that the AAF receiver operates to a nearly closed eye on random data patterns. The mask is split to treat x-1-x (don't care – assertion – don't care) and x-0-x (don't care – negation – don't care) data patterns separately to permit easier testing of a closed eye pattern. The timing for all eye masks is defined by the bit-cell boundaries of the settled 101010 pattern in the de-skew section of the SPI-4 training pattern.

All signal patterns required to test against this input signal specification are included in the Ultra320 training pattern as defined in SPI-4.

All references in the following are to the draft standard SCSI Parallel Interface – 4 (SPI-4) revision 0. That document is available at <ftp://ftp.t10.org/t10/drafts/spi4/spi4r00.pdf>.

Input Signal requirements for a receiver incorporating AAF:

For receivers incorporating AAF compensation, the input signal waveforms shall meet all of the following four amplitude and timing requirements.

1. Low frequency signal amplitude:

The differential low frequency signal amplitude at the receiver during normal data shall fall within the following limits:

$$600\text{mV} < |V_a| + |V_n| < 1.7 \text{ V peak-to-peak}$$

The low frequency signal amplitudes shall be measured after 100 ns continuous assertion (or negation), and may be measured in the training pattern defined in clause 10.8.4.2.

2. Differential Offset:

The differential offset component of the receiver input waveform, defined as the mid-point of the low frequency asserted and de-asserted levels, shall be less than 50 mV.

$$-50 \text{ mV} < [(|V_a| - |V_n|) \div 2] < 50 \text{ mV}$$

3. Free-running clock and settled 1010 pattern amplitude:

The free-running clock and settled 1010 data patterns (1010 patterns preceded by a minimum of 10 bit-cells of 1010 pattern) shall meet the requirements of Mask 1 in Figure 1. This mask is concerned with the "AC" component of the waveform only, and any DC term as calculated in requirement 2 above shall be removed before applying the test mask. The measured data waveform shall be band-limited to 200 MHz.

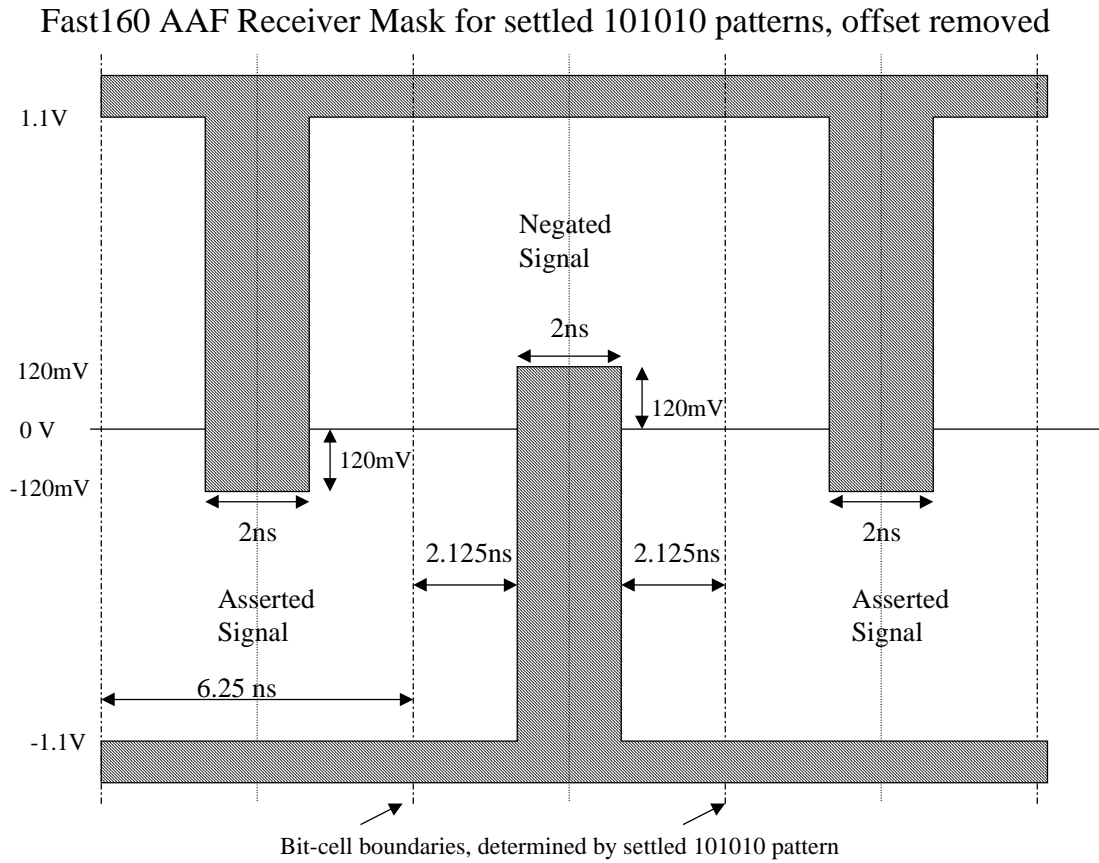
4. All-transitions x0x and x1x masks:

Masks 2a and 2b combined form a traditional eye mask, with limits that permit the eye to be nearly closed. For a negated signal, the receiver input waveform shall exceed 0 volts for 1.5 ns, centered on the bit-cell center as defined by the free-running clock de-skew pattern, as shown in Mask 2a. For an asserted signal, the receiver input waveform shall remain less than 0 volts for 1.5 ns, centered on the bit-cell center.

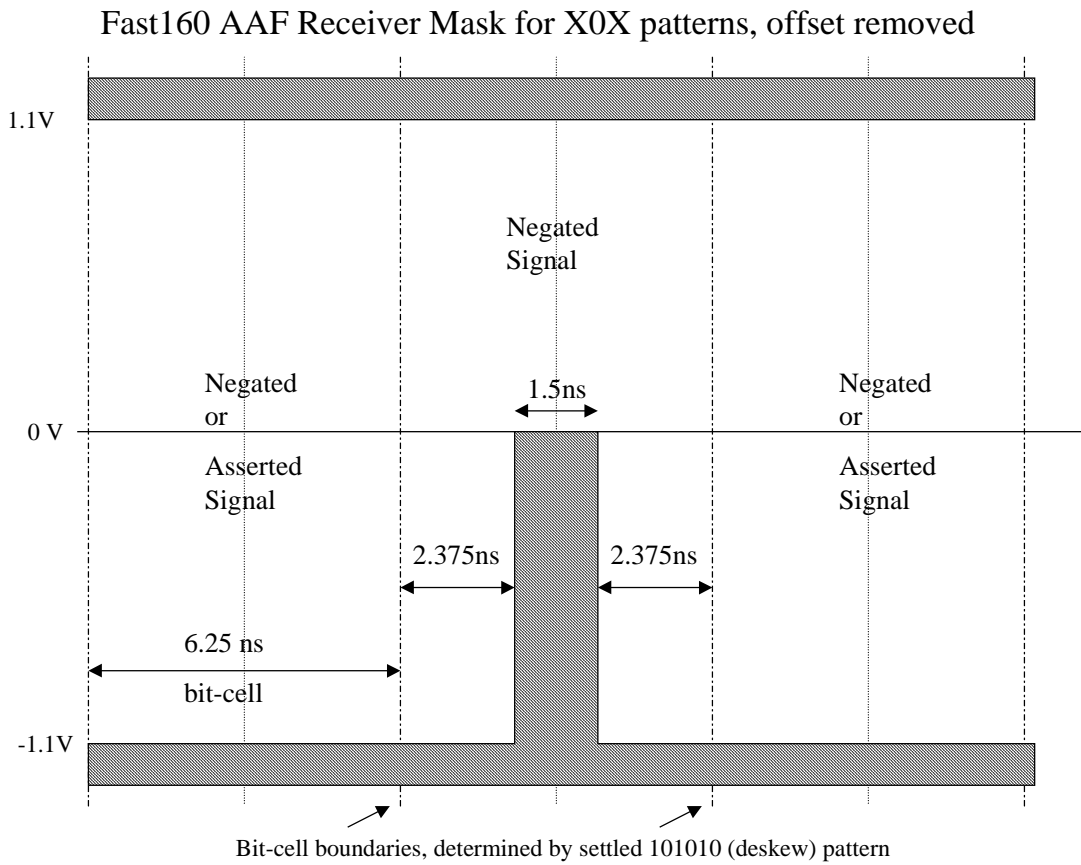
These masks are concerned with the "AC" components of the input waveform only, and any DC term as calculated in requirement 2 above shall be removed before applying the test masks. The measured data waveform shall be band-limited to 200 MHz.

Mask 1 – Free-running clock, and settled 1010 patterns:

A minimum of 10 bit-cells of 1010 pattern must precede the 1010 patterns being tested.



Mask 2a – all x0x transitions:



Mask 2b – all x1x transitions (Mask 2b is a mirror image of Mask 2a):

