Quantum Corporation
500 McCarthy Boulevard
Milpitas, CA 95035 USA

**To:** **T10 Technical committee**
**From:** **Mark Evans**
**Phone: 408-894-4019**
**Email: mark.evans@quantum.com**
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## Subject: Proposal for Ultra320 SCSI timing skew specification for SPI-4

### Introduction

For parallel SCSI transfer rates of 320 megabytes per second, skew compensation must be performed at the receiver on data and clock signals to achieve adequate margin. The following is a concise set of requirements for timing skew for Ultra320 SCSI systems. This proposal specifies only the timing skew requirements between DATA BUS, DB(P1), and REQ(ACK) signals, assuming that other amplitude and timing specifications are provided separately.

The timings in this proposal are derived from the timings in Table 33 in the draft standard SCSI Parallel Interface – 4 (SPI-4) revision 2. All non-compensatable receiver errors in Table 33 are accounted for in this proposal. This accounting does not include REQ(ACK) period tolerance, system noise at launch, and near-end crosstalk as these are not non-compensatable receiver errors. All numbers are listed as ± peak values to clearly indicate symmetrical tolerance around the nominal. SPI-4 rev 2 is available at ftp://ftp.t10.org/t10/drafts/spi4/spi4r02.pdf.

Revision 1 of this proposal addressed comments from the October SPI-4 working group including: doubling the allowable transmitter skew and skew correction range and separating the figures for transmitter time asymmetry and transmitter skew.

Revision 2 of this proposal addresses comments from the January SPI-4 working group including: clarification that the skew correction range is relative to the ACK(REQ) clocking signal. The requirements on the received signal are in clause 9 and do not need to be referenced.

All references in the following are to SPI-4 rev 2.

**The following additions are proposed for Table 32 – SCSI bus data & information phase DT timing values:**

**Table 32 - SCSI bus data & information phase DT timing values**

| Sub-clause | Timing description | Type | Timing Values (note 4) | | | | |
|---|---|---|---|---|---|---|---|
| | | | Fast-10 | Fast-20 | Fast-40 | Fast-80 | Fast-160 |
| | ... | | | | | | |
| 9.2.a | Transmitter skew | max | N/A | N/A | N/A | N/A | ± 0,75 ns |
| 9.2.b | Transmitter time asymmetry | max | N/A | N/A | N/A | N/A | ± 0,25 ns |
| 9.2.c | Skew correction range (see note a) | min | N/A | N/A | N/A | N/A | ± 3,65 ns (see note b) |
| 9.2.d | De-skewed data-valid window (see note a) | min | N/A | N/A | N/A | N/A | ± 2,1 ns |

Note:
a) Measured at the receiver terminal using clean input signals with 500 mV peak amplitude and 1 ns rise and fall time (at 20% to 80%).
b) Relative to the ACK(REQ) clocking signal.

**The following are proposed to be added to clause 9.2**

**9.2.a Transmitter skew**

The maximum difference in time allowed between the rising or falling edge of a "1010…" pattern on the DATA BUS or DB(P1) and its clocking signal on ACK(REQ) as measured at their zero-crossing points. The signals for the output waveforms shall be measured at the connector of the transmitting device under the test conditions as described in A.2.6.

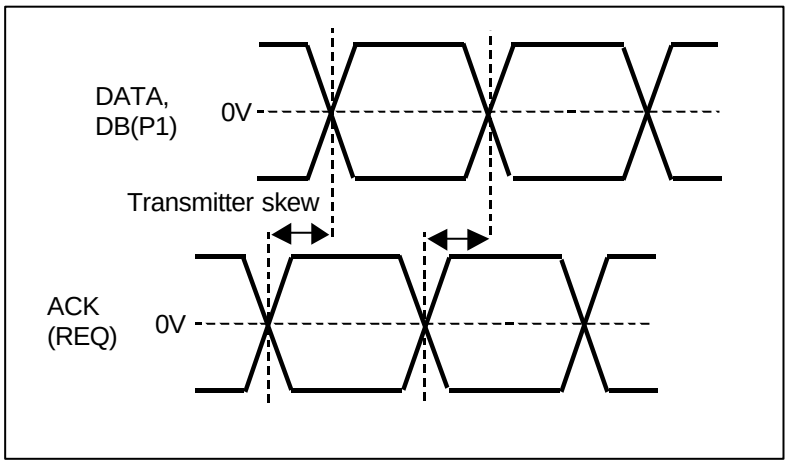


**Figure y – Example of transmitter skew**

**9.2.b Transmitter time asymmetry**

The maximum time on DATA BUS, DB(P1), or ACK(REQ) from any transition edge to the subsequent transition edge during a "1010..." pattern, as measured at their zero-crossing points, minus the data transfer period. The signals for the output waveforms shall be measured at the connector of the transmitting device under the test conditions as described in A.2.6.

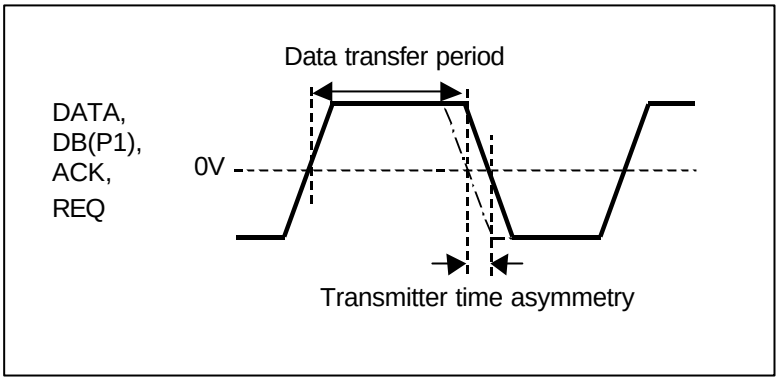


**Figure x – Example of transm itter time asymmetry**

### 9.2.c Skew correction range

The minimum skew correction capability of the receiver of a signal on the DATA BUS or DB(P1) relative to ACK(REQ) as measured at the receiver's connector. The skew correction range shall be equal to ± [ (transmitter chip skew) + (cable skew) + (two times trace skew) ] relative to the corresponding ACK(REQ) clock signal for that transition.. Receiver chip skew is not included, as it is internal to the receiver's ASIC.

### 9.2.d De-skewed data-valid window

The minimum difference in time allowed between the rising or falling edge of a "1010…" pattern on the DATA BUS or DB(P1) and its clocking signal on ACK(REQ) as measured at their zero-crossing points after skew compensation is applied by the receiver without allowing any error in the received data. The de-skewed data-valid window shall be equal to ± [ (data transfer period) – (residual skew error) – (strobe offset tolerance) – (clock jitter) – (receiver amplitude skew) – (chip noise) – (system noise at receiver) – (receiver asymmetry) ] ÷ 2.

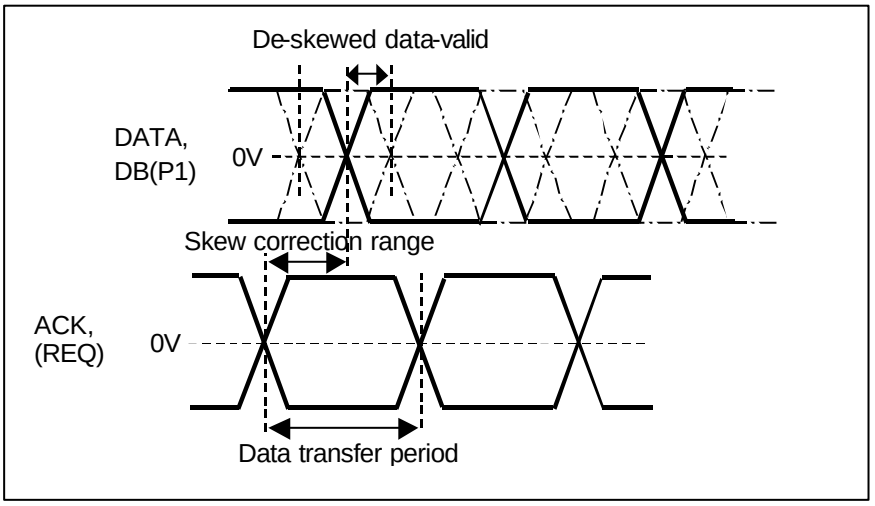


**Figure z – Example of receiver de-skew parameters**