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To: **T10 Technical committee**
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Subject: Proposal for Ultra320 SCSI timing skew specification for SPI-4

Introduction

For parallel SCSI transfer rates of 320 megabytes per second, skew compensation must be performed at the receiver on data and clock signals to achieve adequate margin. The following is a concise set of requirements for timing skew for Ultra320 SCSI systems. This proposal specifies only the timing skew requirements between data bus and REQ/ACK signals, assuming that other amplitude and timing specifications are provided separately.

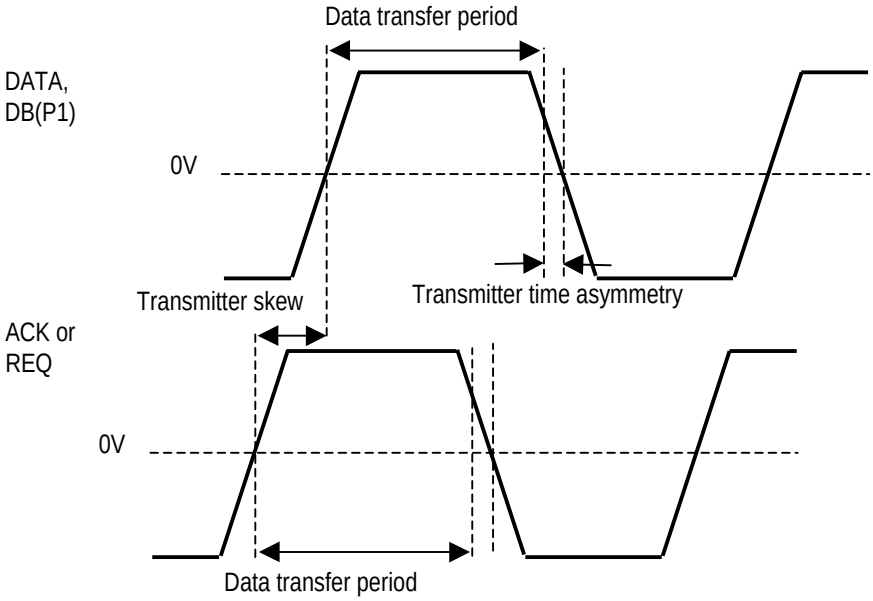
All references in the following are to the draft standard SCSI Parallel Interface – 4 (SPI-4) revision 0. That document is available at ftp://ftp.t10.org/t10/drafts/spi4/spi4r00.pdf.

Timing skew test conditions:

a) An alternating "1010…" pattern on the data line,
b) Test transmitter signals with ideal loads (according to the test circuit of Figure A.7 – Differential output switching voltage test circuit),
c) Test receiver with ideal input signals of 500 mV_{peak} and 1 ns (20% to 80%) rise and fall time (see A.3.4 Receiver setup and hold times),
d) Skew correction range specifies minimum skew correction capability at the receiver's pins including transmitter chip skew, cable skew and two times trace skew as defined in Table 33 (receiver chip skew is not included, as it is internal to the receiver chip),
e) De-skewed data-valid window is the minimum tolerable time shift between the data and ACK (REQ) signals after skew compensation.
f) All non-compensatable receiver errors in Table 33 are accounted for in this proposal.
g) All numbers are listed as ± peak values to clearly indicate symmetrical tolerance around the nominal point.

Transmitter skew specifications

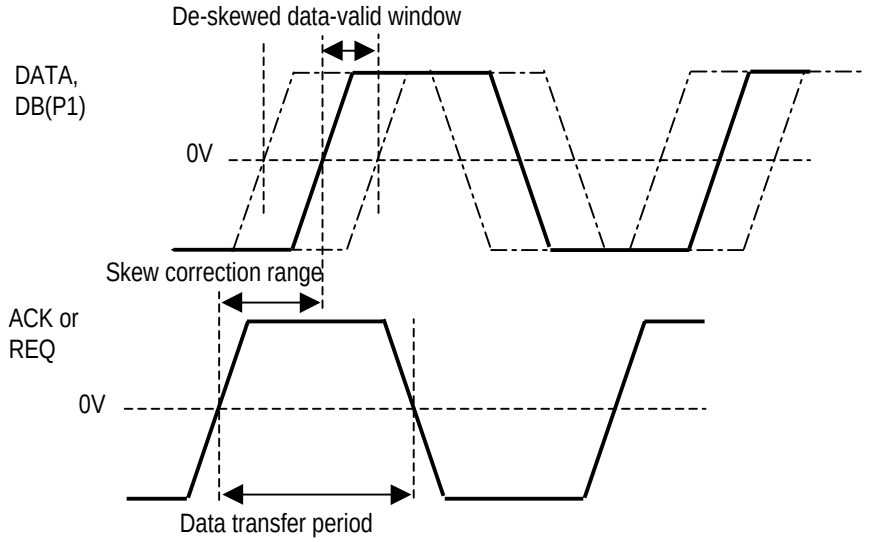
Item	Proposed Spec	Comments
Transmitter skew	± 0.375 ns	Max skew between databus & ACK (REQ)
Transmitter time asymmetry	± 0.25 ns	Max duty-cycle error on databus & ACK (REQ)
Note: Timing is measured at the zero-crossing points for waveforms under the test conditions as described in A.2.6 Output signal waveform.		



Receiver de-skew specifications

Item	Proposed Spec	Comments
Skew correction range[2]	± 1.825 ns	Min skew correction capability at the receiver
De-skewed data-valid window[3]	± 2.1 ns	Min tolerable skew after calibration

Notes:
1 Timing is measured at the zero-crossing points for waveforms under the test conditions as described in A.2.6 Output signal waveform and ideal input signals with 500mVp amplitude and 1ns rise and fall time (20% to 80%).
2 Skew correction range = ± [(transmitter chip skew) + (cable skew) + (2 x trace skew)] ÷ 2
3 De-skewed data-valid window = ± [(data transfer period) – (residual skew error) – (strobe offset tolerance) – (clock jitter) – (receiver amplitude skew) – (chip noise) – (system noise at receiver) – (receiver asymmetry)] ÷ 2.



The following modifications are proposed for Table 32:

Table 32 - SCSI bus data & information phase DT timing values

Subclause	Timing description	Type	Timing Values (note 4)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
	...						
	Transmitter Skew	max	N/A	N/A	N/A	N/A	± 0,375 ns
	Transmitter Time Asymmetry	max	N/A	N/A	N/A	N/A	± 0,25 ns
	Skew Correction Range (Note b)	min	N/A	N/A	N/A	N/A	± 1,825 ns
	De-skewed Data-valid Window (Note b)	min	N/A	N/A	N/A	N/A	± 2,1 ns

Notes:
a. Calculated assuming timing budget shown in table 33.
b. Measured at the receiver terminal using clean input signals with 500mVp amplitude and 1 ns rise and fall time (at 20% to 80%).