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10/31/2000
John Lohmeyer
T10 Chairman

Subject: Proposal to replace the TBDs for Fast 160 in SPI-4 and to winnow the options

The September meeting of T10 admonished the working group to reduce the optional analog requirements for Fast 160 before replacing the remaining TBDs. This proposal does both. For the most part this proposal is a repeat of the content of T10/99-295r5 that was recommended by the working group before values within it were replaced in SPI-4r0 by TBDs. Considerable testing as shown in presentations by Bruce Manildi and John Masiewicz to the various ad hoc meetings continues to support the proposed values as well as confirming better results with SPI-4 compliant drivers as opposed to the driver characteristics available so far in the more general purpose test equipment.

The 10/31/2000 working group that recommended changes to 00-389r0 and recommended that T10 approve the proposal as modified in revision 1 to be included in the next revision of SPI-4 asked for the changes in part due to the proposer's error in using a SPI-3 file as the basis for some portions of that revision. (The principal reason for some deleted portions of the proposal was that they were already in SPI-4 Rev 0 in an equivalent manner.) In addition to the changes recommended by the working group the additional example receiver masks that were included for illustrative purposes in presentation of the proposal but not for inclusion in SPI-4 have been deleted.

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p.s. Although the SPI-3 files were used, clause numbers, figure numbers, and table numbers are as FrameMaker determined and have not been synchronized to SPI-4.

9.3.4 LVD measurement points

(Skip the timing figure stuff and then:)

Figure 50 shows the LVD signal requirements at the receiving SCSI device with synchronous transfers. During paced transfers with precompensation-enabled SCSI devices shall operate with signals at the receiving SCSI device meeting either figure 51, figure 52, or both. Mask ± 2 is applicable to signals that have more timing margin than those for mask ± 1 and allows less amplitude margin than does mask ± 1 . The lower amplitude margin of mask ± 2 may result in timing margin loss internal to the receiver but is accounted for in the timing budget. The higher amplitude margin of mask ± 1 should result in less timing margin loss internal to the receiver. For the cases where the data signal remains at a particular bit state without transitions for more than one transfer period, these masks include a variable asserted or negated period as a function of n (the number of transfer periods with adjacent data at the same state).

Editor's note: In preparing the changes from the working group meeting I noticed that somewhere along the line Mask 1 and Mask 2 were interchanged. Making the above number changes seemed to involve the fewest changes in revision 1 of this proposal. But for inclusion in SPI-4 the choice is somewhat arbitrary as long as the descriptive text matches the chosen order (mask number).

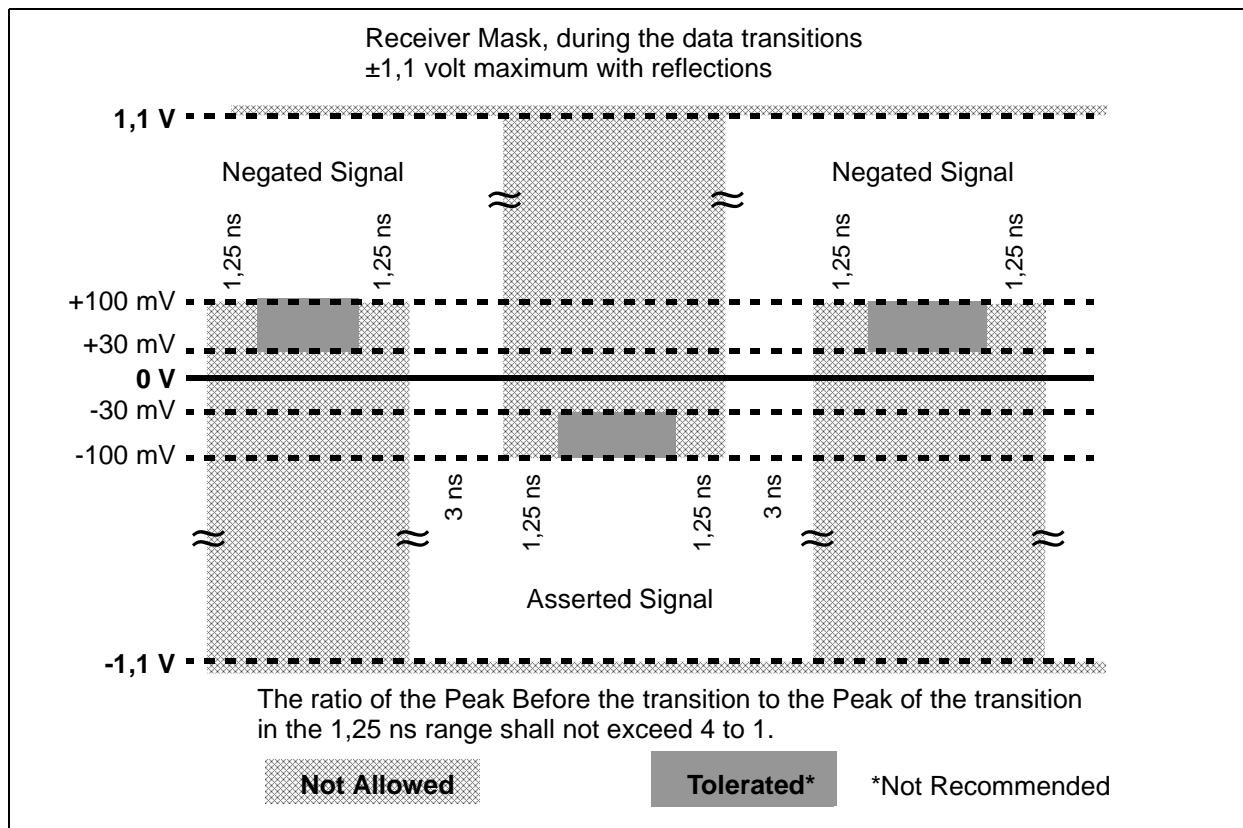


Figure 50 - LVD receiver mask \leq Fast 80

For Fast 80 the signal shall transition from -100 to +100 mV or +100 to -100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. The absolute value of the signals shall remain above the 100 mV level for 1,25 ns at each end of the transition. The absolute value of the signals shall not drop below 30 mV except during the transitions (see 7.3.2).

Proposer's note: The above text has been moved from below Figure 49 to below Figure 50.

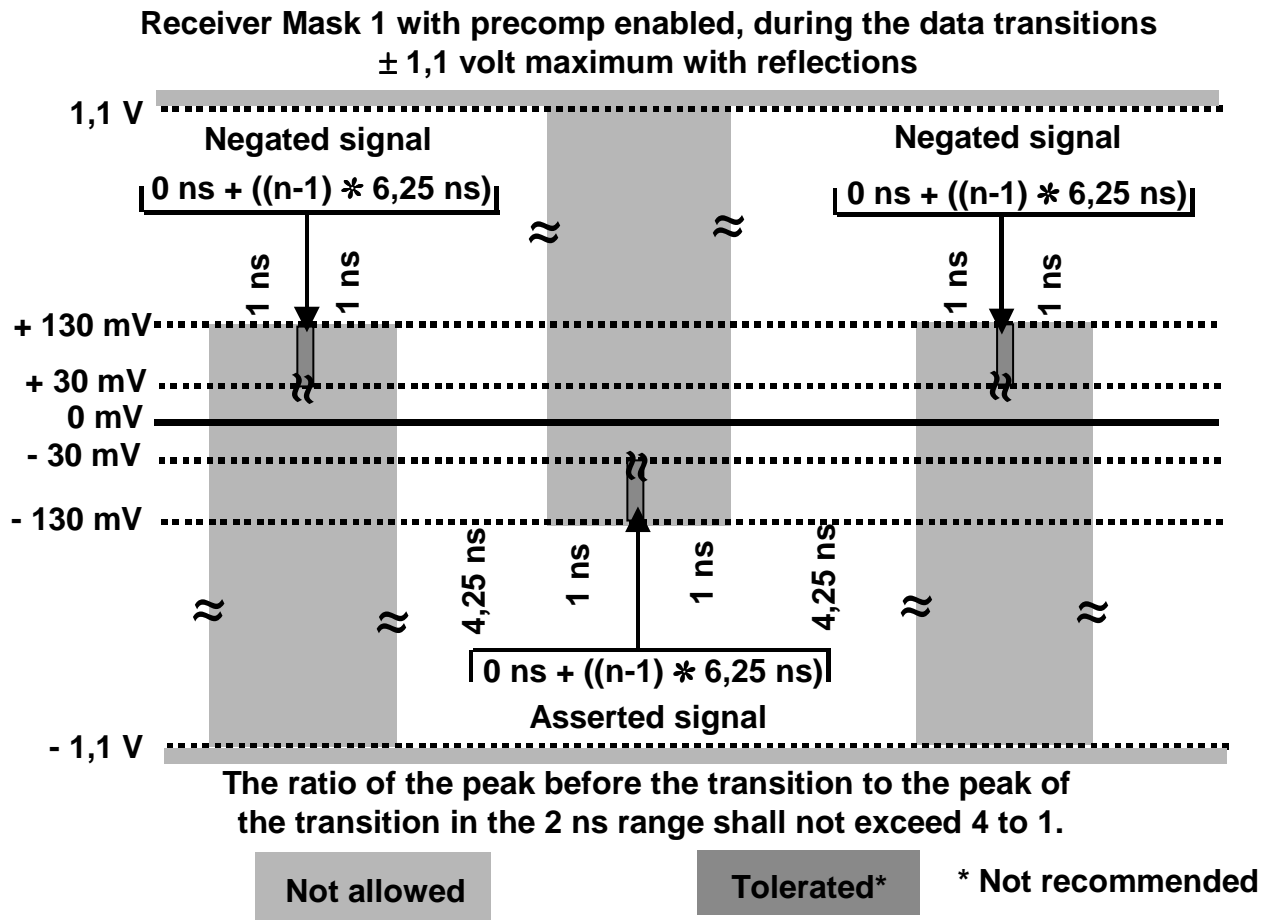


Figure 1 - LVD receiver mask 1 = Fast 160

Proposer's note: This is Figure 51.

For Fast 160 the signal shall transition from -130 to +130 mV or +130 to -130 mV in 0 to 4,25 ns, the waveform between -130 and +130 mV is not otherwise specified. The absolute value of the signals shall remain above the 130 mV level for 1 ns at before and after each transition.

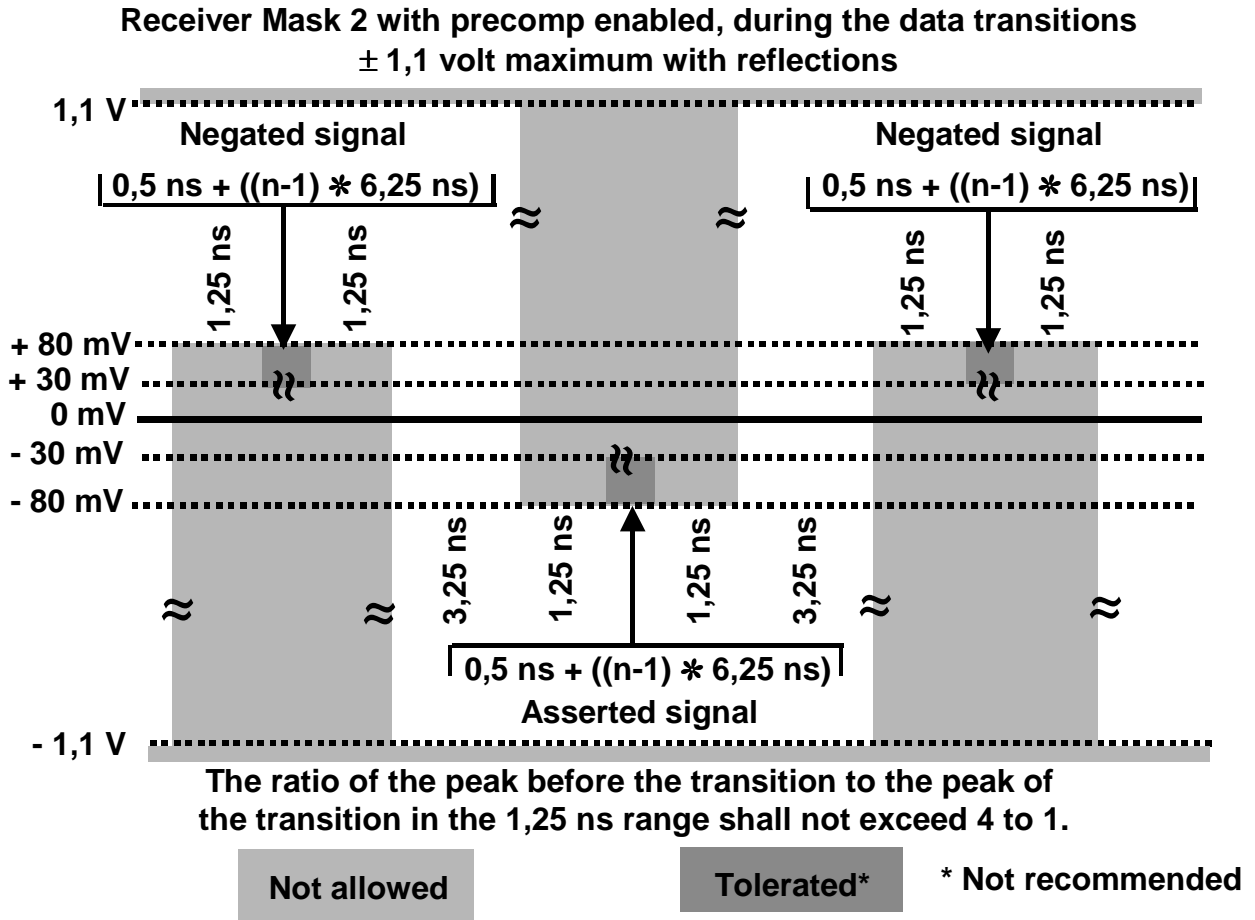


Figure 2 - LVD receiver mask 2 = Fast 160

Proposer's note: This is Figure 52.

Alternatively, for Fast 160 the signal shall transition from - 80 to + 80 mV or + 80 to - 80 mV in 0 to 3,25 ns, the waveform between - 80 and + 80 mV is not otherwise specified. The absolute value of the signals shall remain above the 80 mV level for 1,25 ns before and after each transition. The absolute value of the signals shall not drop below 30 mV except during the transitions (see 7.3.2).

Annex A Additional requirements for LVD SCSI drivers and receivers

(normative)

A.1 System level requirements

The requirements for LVD SCSI drivers and receivers in this annex are based on the system level requirements stated in table A.1. Some of these requirements are specifically called out in other subclauses while others are derived from bus loading conditions and trade-offs between competing parameters.

Table A.1 - System level requirements

Parameter	Minimum	Maximum	Cross-reference
V_A (except OR-tied signals)	-1 V	- 100 mV	<Fast 160 note 1
V_A (except OR-tied signals)	-1 V	- 80 mV	Fast 160 note 1
V_N (except OR-tied signals)	100 mV	1 V	<Fast 160 note 1
V_N (except OR-tied signals)	80 mV	1 V	Fast 160 note 1
V_A (OR-tied signals)	-3,6 V	- 100 mV	note 1
V_N (OR-tied signals)	80 mV	145 mV	note 1, 5
attenuation (%)	N/A	45	<Fast 160 note 2
attenuation	N/A	3 dB at 80 MHz	Fast 160 note 2
loaded media impedance (Ohms)	85	135	note 3
unloaded media impedance (Ohms)	110	135	subclause 6.3
terminator bias (mV)	100	125	subclause 7.3.1
terminator impedance (Ohms)	100	110	subclause 7.3.1
device leakage (μ A)	-20	20	table 16
number of SCSI devices	2	16	subclause 4.7
ground offset level (mV)	-355	355	note 4
<p>Note:</p> <p>1 -These are the signal levels at the receiver, the system allows 60 mV crosstalk for calculating the minimum driver level.</p> <p>2 - Measured from the driver to the farthest receiver.</p> <p>3 -Caused by the addition of device capacitive load (see table 9 for calculations).</p> <p>4 -This is the difference in voltage signal commons for SCSI devices on the bus (see figure 3).</p> <p>5 - SPI standards prior to this standard did not account for leakage current.</p>			

Proposer's note: The working group requested that the attenuation rows be removed in favor of a future document that the PIP working group is attempting to produce.

A.2 Driver requirements

A.2.1 Driver requirements overview

The fundamental requirement for an LVD driver is the generation of a first-step differential output voltage magnitude at the driver connections to the balanced media to achieve required minimum differential

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signals at every receiver connection to the bus. If a P_EN bit of one was received by a SCSI device during the prior PPR negotiation, the weak driver amplitude shall be a minimum of 50% to a maximum of 66% of the strong driver amplitude after the first bit of a series of adjacent ones or adjacent zeros. Other characteristics that affect overall noise margin are the common-mode output voltage, the maximum differential output voltage, the driver output impedance, and the output signal wave shape.

NOTE 19 - If a weak driver is driving with the minimum amplitude specified in table A.2, then the 370 mV weak driver translates to a strong driver of 560 mV for the 66% case ranging up to 740 mV for the 50% case.

The driver requirements are defined in terms of the voltages and currents depicted in figure 43.

Table A.2 - Driver steady-state test limits and conditions and alternating 1/0 data transfer phase

Test parameter	Test conditions (figure A.1) ¹	Minimum (mV) Fast < 160	Minimum (mV) ² Fast 160	Maximum (mV) Fast =< 160
V _A Differential output voltage magnitude (asserted) (note)	V ₁ = 1,056 V V ₂ = 0,634 V	320	370	800
	V ₁ = 1,866 V V ₂ = 1,444V	320	370	800
V _N Differential output voltage magnitude (negated) (note)	V ₁ = 1,056 V V ₂ = 0,634 V	320	370	800
	V ₁ = 1,866 V V ₂ = 1,444V	320	370	800
Fast < 160 V _A Differential output voltage magnitude (asserted)	All four above conditions	0,69 x V _N + 50	N/A	1,45 x V _N - 65
Fast 160 V _A Differential output voltage magnitude (asserted)	All four above conditions	N/A	(0,9 x V _N) - 23	(1,11 x V _N) + 26
Notes: 1) The test circuit (figure A.1) is approximately equivalent to two terminators creating the normal system bias. 2) Including cutback. 3) The test limits shall be within the shaded domain of Figure A.2.				

A.2.2 Differential output voltage, V_s

This subclause does not specify requirements for drivers with source impedances less than 1000 Ohms.

To assure sufficient voltage to define a valid logic state at any device connection on a fully loaded LVD bus at least a minimum differential output voltage shall be generated. This value shall be large enough that, after allowance for attenuation (~~AC and DC~~), reflections, terminator bias difference, and differential noise coupling, V_s is at least +100 mV meets the specified requirements at the device connector to the LVD SCSI bus.

The SCSI device shall also comply with the upper limits for the differential output voltages and to the symmetry of the differential output voltage magnitudes between logic states in order to assure a first-step transition to the opposite logic state.

With the test circuit of figure A.1 and the test conditions V₁ and V₂ in table A.2 applied, the steady-state magnitude of the differential output voltage, V_S, for an asserted state (V_A), shall be greater than or equal to 320 mV for Fast < 160 or 370 mV for Fast 160 and less than or equal to 800 mV. For the negated state, the polarity of V_S shall be reversed (V_N) and the differential voltage magnitude shall be greater than or equal to 320 mV for Fast < 160 or 370 mV for Fast 160 and less than or equal to 800 mV. The relationship between V_A and V_N specified in table A.2 and shown graphically in figure A.2 for Fast < 160 and in figure A.3 for Fast 160 shall be maintained.

The assertion drivers and negation drivers require different strengths to achieve the near equality in V_A and V_N shown in figure A.2 and A.3 because the applied V₁ and V₂ simulate the effects of the bus termination bias.

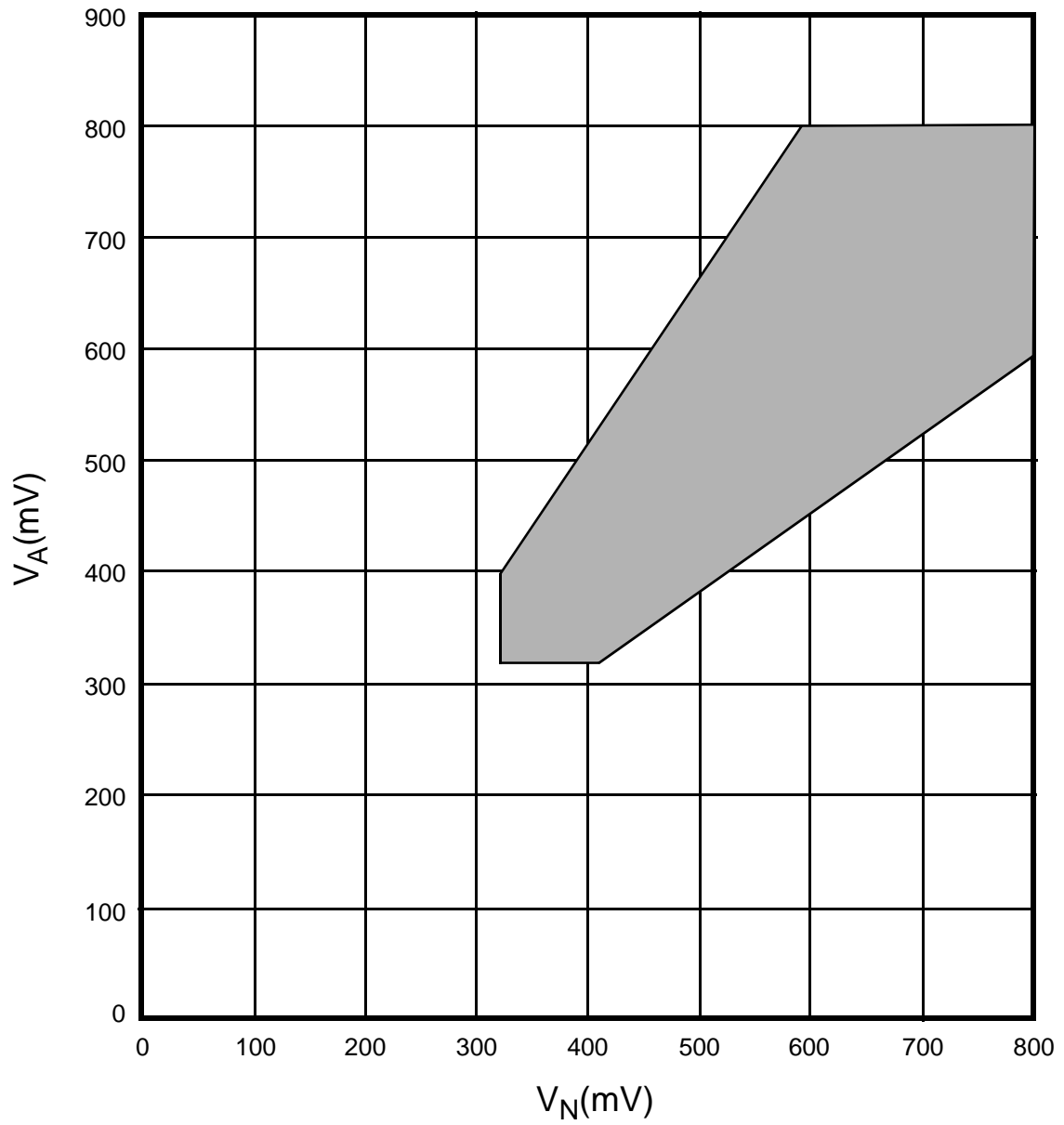


Figure A.1 - Domain for driver assertion and negation levels for Fast <160

Proposer's note: The above figure should be Figure A.2.

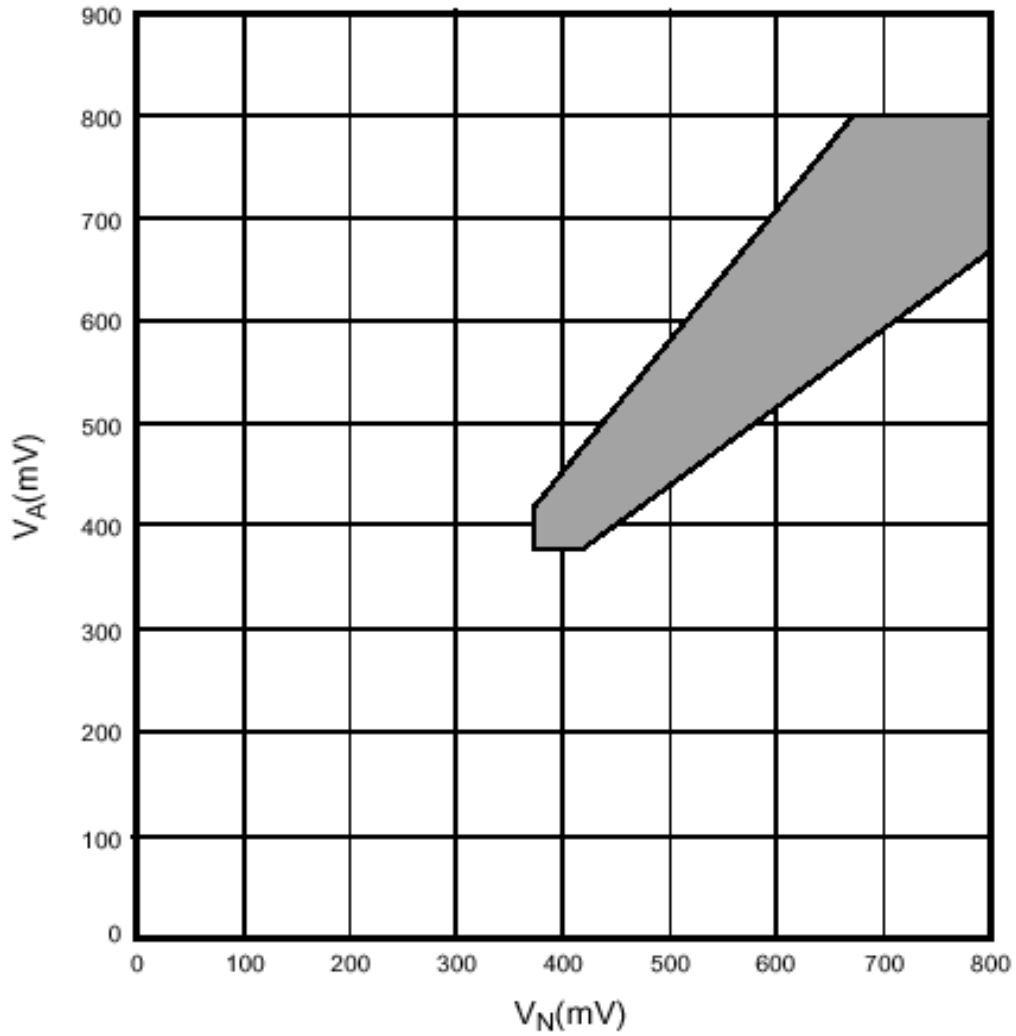


Figure A.2 - Domain for driver assertion and negation levels for Fast 160

Proposer's note: The above figure should be Figure A.3.