T10/00-353r0

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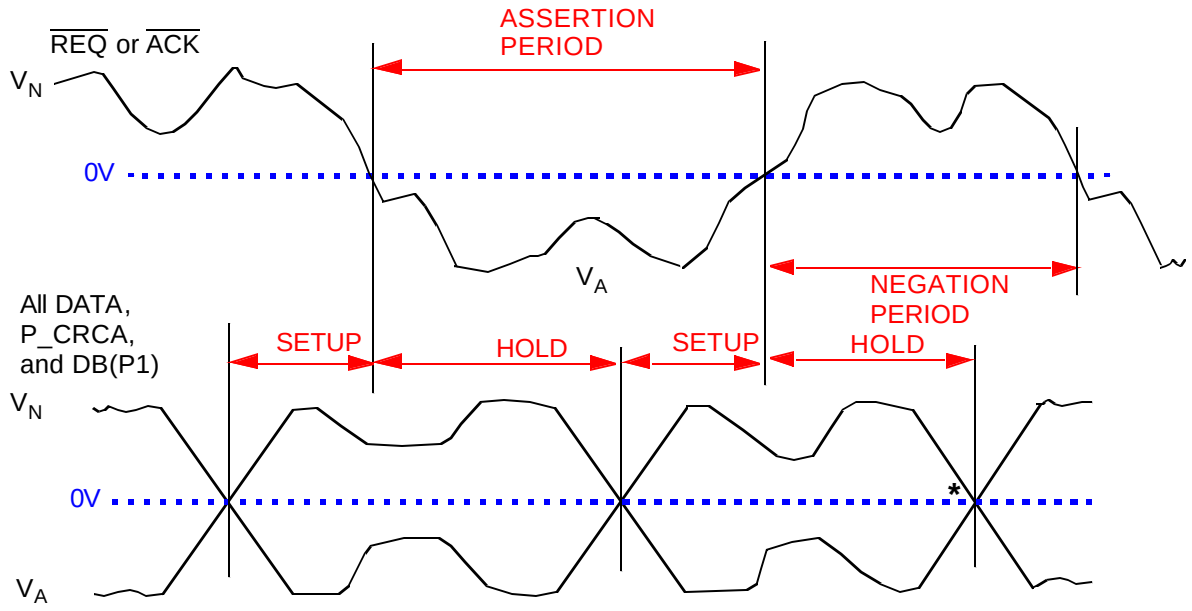
9/12/2000
John Lohmeyer
T10 Chairman

Subject: **Proposal for revised setup and hold figures to be included in SPI-4**

The attached figures have been described and I think agreed to in various working groups as word pictures. This proposal documents the word pictures in FrameMaker.

Gene Milligan
Director, Development Strategy
Seagate Technology Inc.



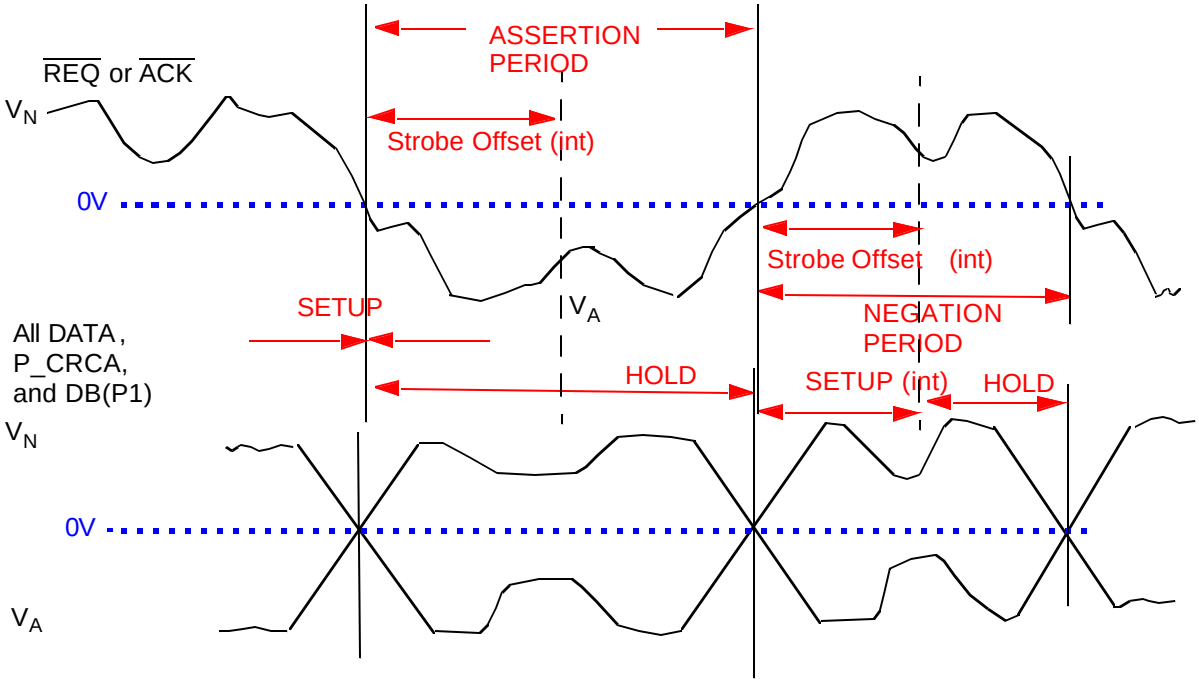
Notes:
1 V_N - negated signal
2 V_A - asserted signal
3 ~~t_m = 1,25ns minimum~~
4 ~~V_A or V_N are required to drive the 100 mV at the leading edge of the transition. Those signals shall be at least |100 mV| for at least t_m before and after the transition.~~
5 Differential voltage signals in all cases.
6 ~~t_{af} and t_{ar} shall be less than 3 ns.~~
7 ~~Any signal structure may occur at the receiver while in the t_{af} or t_{ar} region including slope reversal.~~

Figure 42 - LVD timing measurement points for DT =< Fast-80 data transfers

The signal shall transition from -100 to +100 mV or +100 to - 100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. Signals shall remain above the |100 mV| level for 1,25 ns at each end of the transition. The signals shall not drop below |30 mV| except during the transitions. Conditions exist with longer, loaded SCSI busses and irregular REQ and ACK pulse widths where long assertions or negations produce a much larger signal than short assertions or negations. This sets up an environment where the short REQ or ACK pulses may not have adequate timing margin unless the definitions in figure 44 are used in the measurement of timing parameters. If the P_EN bit equals one precompensation mitigates the charging effect and helps timing margin.

Measurement of driver timing parameters shall be performed using the circuit and test conditions defined in A.2.5 applied to the SCSI device connector. Receiver timing parameters are defined by the waveforms existing at the connector of the receiving SCSI device. The receiver timing parameters include the effects of data pattern. The receiver data pattern is therefore not defined.

Figure 46 shows the LVD signal requirements at the receiving SCSI device.



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7 Any signal structure may occur at the receiver while in the t_{af} or t_{ar} region including slope reversal.

8 Strobe Offset is from the actual detected time to the implemented offset time. (int) = internal. Since effective timing is based upon actual detection, all timing measurements shall be based upon zero crossings for Fast 160.

Figure 43 - LVD timing measurement points for DT = Fast - 160 data transfers