Quantum™

T10/00-331r0

Losses on LVD Buses

Richard Uber
Quantum Corporation

August 24, 2000

Quantum™

D.C. Noise Margin Factors

- Several factors are not being taken into account for Ultra320 SCSI D.C. noise margin analyses:
  - Bus offset variations related to non-ideal terminators
  - Bus offset variations due to D.C. resistance of the bus
  - V_A and V_N range and mismatch from wedge shaped plot in figure A.2 in Appendix A
  - Driver cutback ratio
  - Tolerance of cutback ratio

Bias Cancellation Current

There are at least 3 definitions for "nominal bias cancellation current":

1) The current required to get balanced assertion and negation voltages with the ideal load circuit as described in Appendix A in SPI-4.

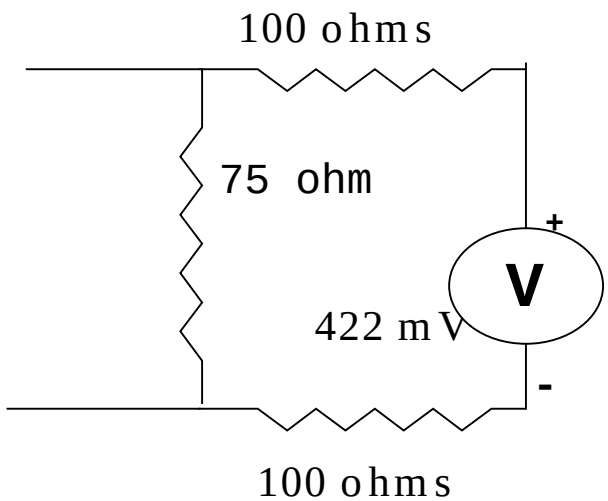
2) The current which minimizes D.C. errors with the whole range of allowed terminators on a short bus.

3) The current which minimizes D.C. errors with the whole range of allowed terminators on a long bus.

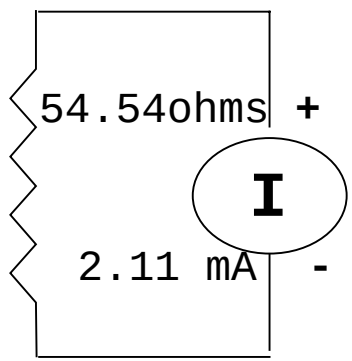
Quantum™ Standard LVD Test Load SPI-2, -3, -4

- Specified LVD Driver Load circuit (V, R)
- Load can be expressed as current source equivalent (I,R)

Standard Test Load



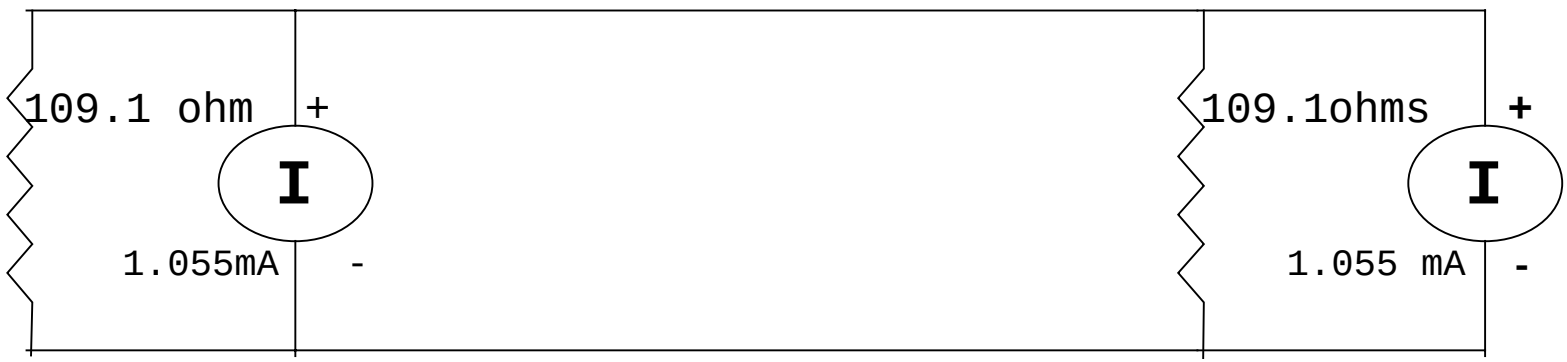
Equivalent Current Load



Bus with "Nominal" Terminators

- The figure below shows a standard load broken in half and placed at the ends of a SCSI bus.
- The negation bias is perfectly cancelled for an ideal load when the driver assertion current is 2.11 mA larger than the driver negation current.
- Ideal terminator parameters are:
  - 109.1 Ω resistance
  - -1.055 mA D.C. current
  - -115.1 mV D.C bias

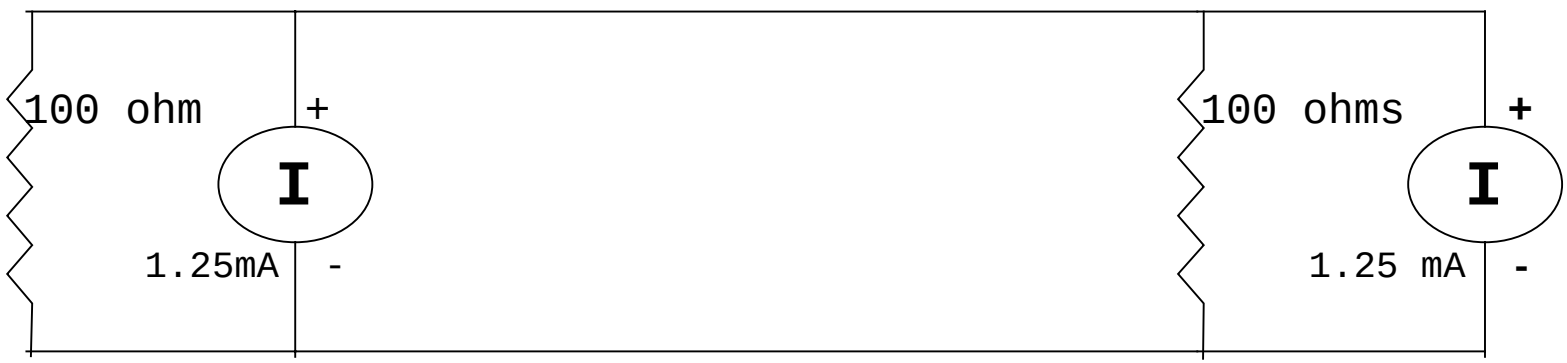
Nominal bus, terminators = "half a Standard load"



Max Negation Current Terminator

- Terminator parameters should be chosen to maximize negation current.
- Negation bias is perfectly cancelled when driver assertion current is 2.50 mA larger than driver negation current.
- A bias cancellation current of 2.11 mA yields a current offset of -0.39 mA, or -19.5 mV
- Max negation current terminator parameters are:
  - 100 Ω Resistance
  - -1.25 mA D.C. current
  - -125 mV D.C bias

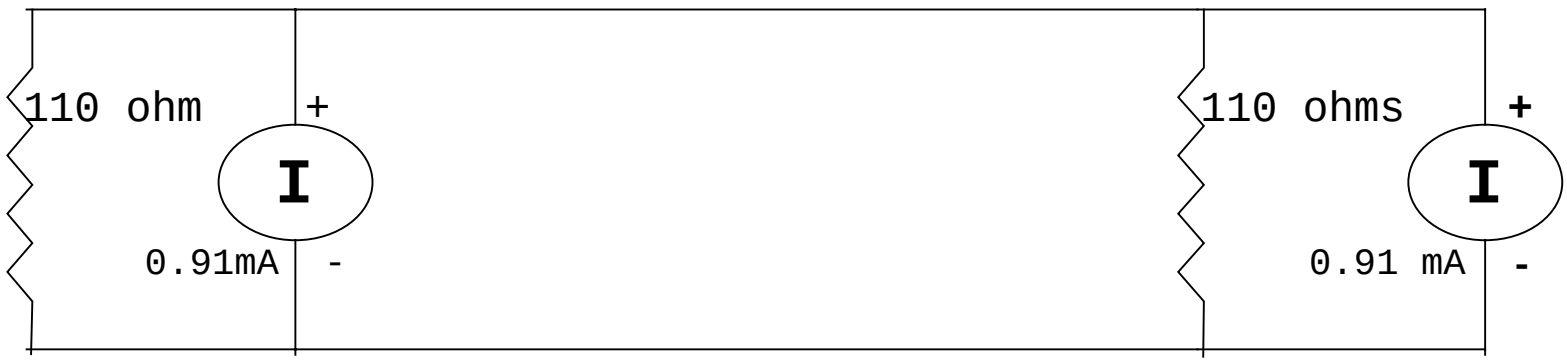
Max current terminator forces a stronger negation



Min Negation Current Terminator

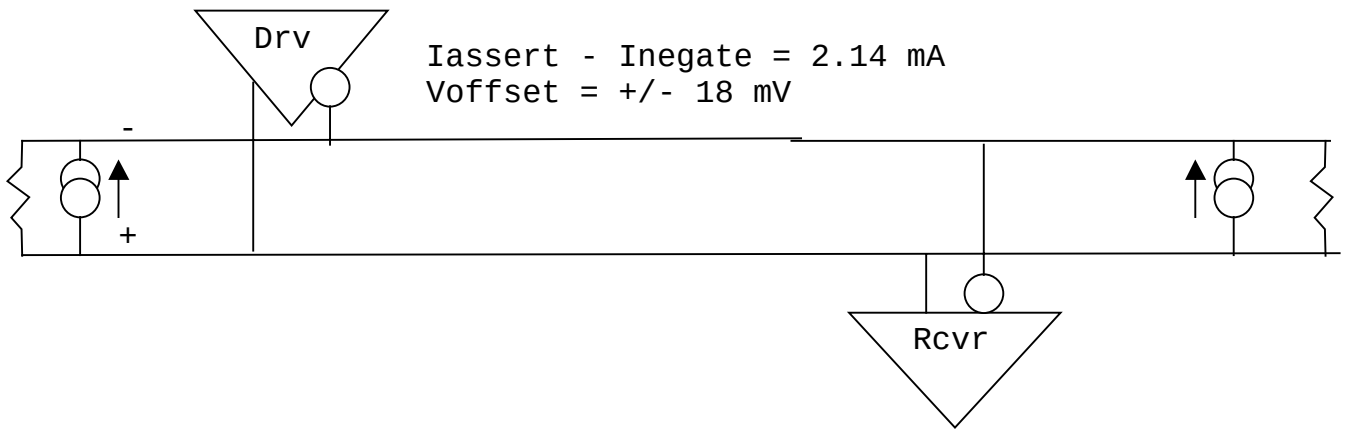
- Terminator parameters should be chosen to minimize negation current.
- Negation bias is perfectly cancelled when driver assertion current is 1.82 mA larger than driver negation current.
- A bias cancellation current of 2.11 mA yields a voltage offset of +0.29 mA, or +16.1 mV.
- Min negation current terminator parameters are:
  - 110 Ω Resistance
  - -0.91 mA D.C. current
  - -100 mV D.C bias

Min current terminator forces a weaker negation



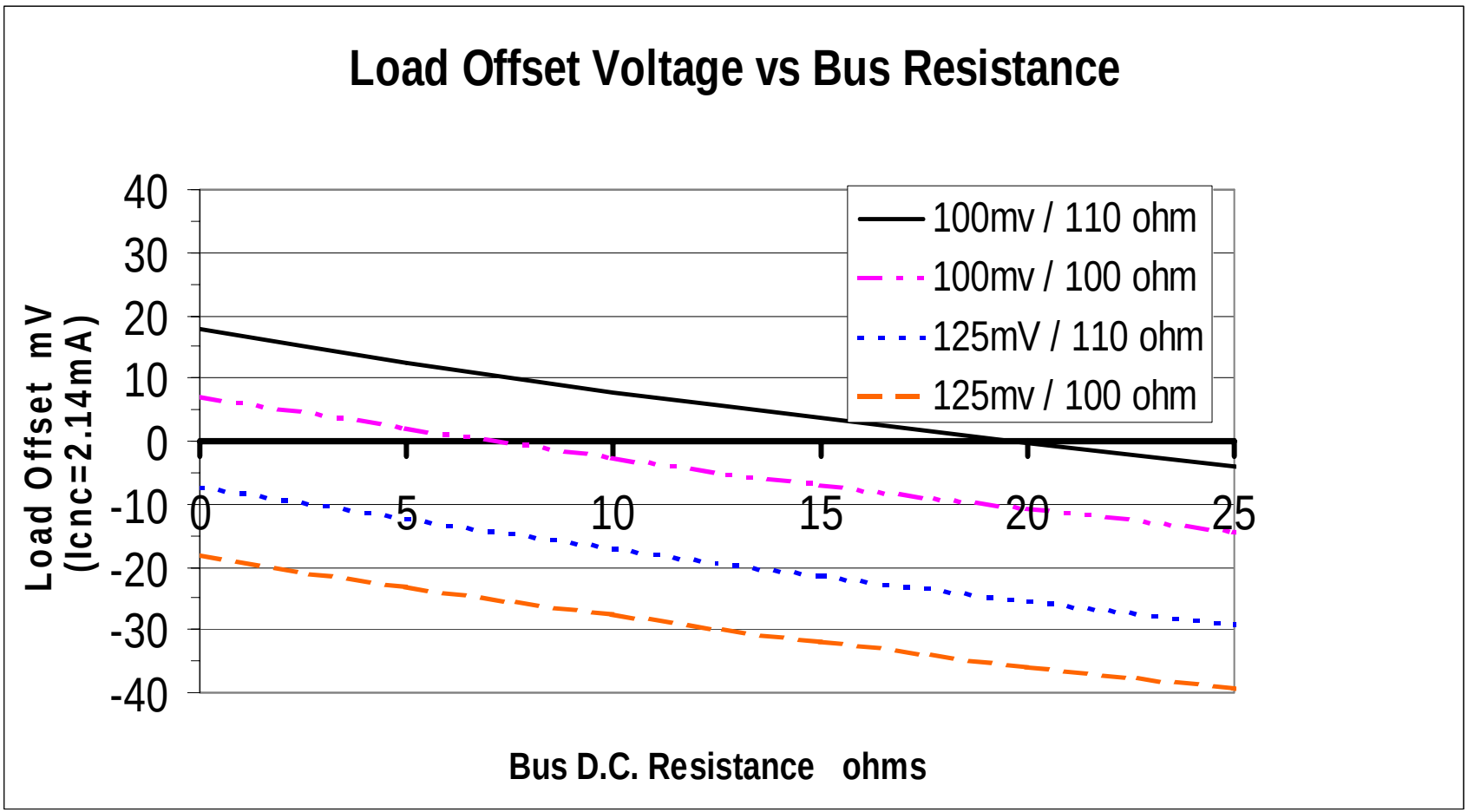
Short Bus Min Terminator Offsets

- The standard load is perfectly balanced with 2.11 mA, but that is not matched to the range of terminator currents.
- I_{cnc} = 2.11 mA yields a -19.5 mV error on strong terminators
- I_{cnc} = 2.11 mA yields a +16.1 mV error on weak terminators
- A target I_{cnc} of 2.14 mA balances the strong and weak terminator errors:
  - Strong case: (2.14 mA - 2.50 mA) * 50 Ω = +18 mV
  - Weak case: (2.14 mA - 1.82 mA) * 55 Ω = -18 mV



Bus Resistance Offsets

- A bias cancellation current which provides perfect balance on a short bus will result in a negation bias at the load if there is a bus resistance between the source and the load.

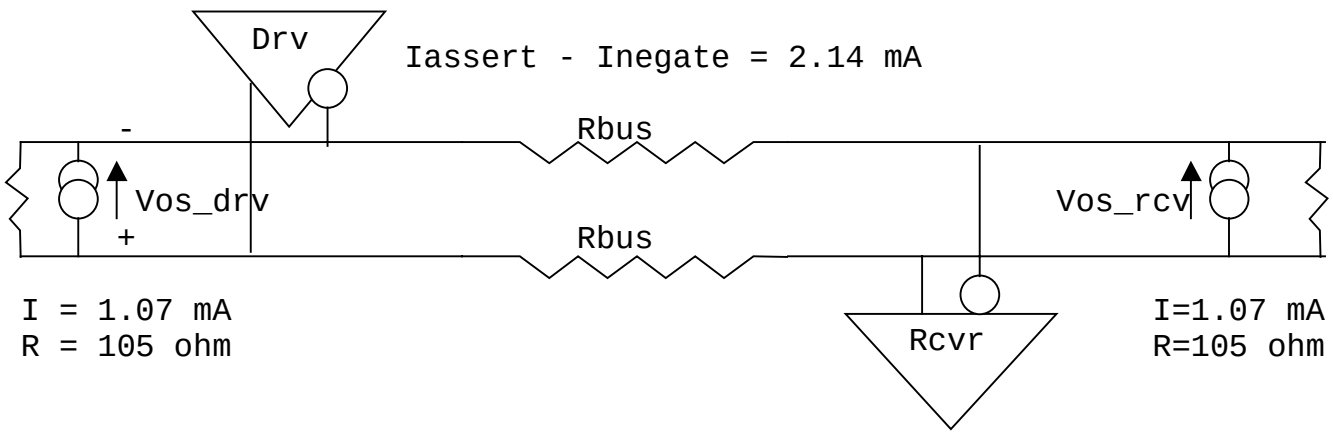


Bus Resistance Affects Offsets

- Adding D.C. bus resistance between the driver and the receiver unbalances the terminator cancellation current.
- The offset at the driver will move towards assertion.
- The offset at the receiver will move towards negation.
- Optimal driver balance is not at zero, but at a slight assertion bias.

For Rbus = 0 Ω,
Vos_drv = 0 mV
Vos_rcv = 0 mV

For Rbus = 10 Ω,
Vos_drv = +10 mV (assertion)
Vos_rcv = -10 mV (negation)

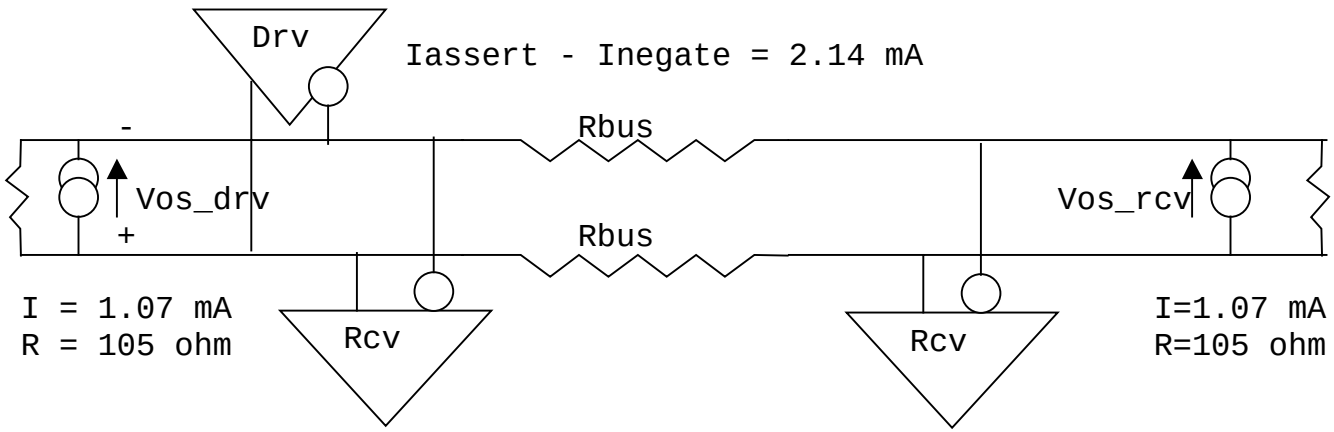


Resistive Bus Offset Equations

- Bias cancellation current, $I_{cnc} = I_{assertion} - I_{negation}$
- $I_{term\_near} = V_{term\_near} / R_{term\_near}$
- $I_{term\_far} = V_{term\_far} / R_{term\_far}$
- R_{bus} = D.C. resistance of each conductor in a bus
- $Z@drvr = R_{term\_near} // (R_{term\_far} + 2 * R_{bus})$
  $= R_{term\_near} * (R_{term\_far} + 2*R_{bus}) / (R_{term\_near} + R_{term\_far} + 2*R_{bus})$
- $Z@rcvr = R_{term\_far} // (R_{term\_near} + 2*R_{bus})$
  $= R_{term\_far} * (R_{term\_near} + 2*R_{bus}) / (R_{term\_far} + R_{term\_near} + 2*R_{bus})$
- $V_{offset\_rcvr} = (I_{cnc} - I_{term\_near}) * Z@drvr * (R_{term\_far}) / (R_{term\_far} + 2 * R_{bus}) - I_{term\_far} * Z@rcvr$
- $V_{offset\_rcvr} = -V_{offset\_drvr}$ (for most distant load)
- $V_{offset\_rcvr} = V_{offset\_drvr}$ (for an adjacent load)

Bus Topology Affects Offsets

- If the bus resistance is between the source and load, then biasing the bus towards assertion will improve balance.
- Many applications have all initiators at one end of the bus and all targets at the other. If the dominant bus resistance is in the cable, then over compensating for the terminator bias (towards assertion) will improve balance.
- If the bus is homogeneous (loads and resistance evenly distributed) then any adjustment to bias cancellation current will result in degraded margin at one of the extreme loads.



Optimal Bias Cancellation Currents

- I_{cnc} = 2.11 mA for the specified ideal LVD load circuit.
- I_{cnc} = 2.14 mA for short (low resistance) buses with the full range of allowed terminator characteristics.
- $I_{cnc} = F(R_{bus}, I_{term}, R_{term})$ for buses with all initiators separated from all targets by R_{bus}. Biasing the bus towards assertion will reduce the worst case offset.
- Icnc = 2.14 mA for buses with targets (or initiators) on both sides of the bulk of the bus resistance. In this case, the D.C. offset errors cannot be compensated for with a single driver setting.

D.C. Losses Summary

- +26 / -23 mV budget for canceling out the terminator negation bias current [$I_{cnc} = -I_{term} = (I_{assert} - I_{negate})$] when driving an ideal load, per Appendix A (also see 00-319r0).
  - Included in Figure A.2
- +/- 18 mV budget for differences between the ideal load and the terminator extremes of bias current.
  - Not included in Figure A.2
  - Must be considered in calculating first pulse noise margins.
- +0 / -30 mV offset for bus D.C. resistance.
  - Not included in Figure A.2.
  - Topology dependent.
  - If the bulk of the bus resistance separates all initiators from all targets, then forcing the assertion voltages to be larger than the negation voltage by half of the offset will improve worst case balance.
  - Must be considered in calculating first pulse noise margins.

A.C. Noise margin factors

- Several factors are not being taken into account for Ultra320 SCSI A.C. noise margin analyses:
  - Adjusting (current mode) driver output voltage to reflect the actual bus impedance relative to standard load
  - Bus signal losses due to attenuation
  - Reflection losses at impedance discontinuities
  - First pulse shape distortion due to ISI (frequency dispersion) on cable

Quantum™

Target Output Swing Into Backplane

- LVD signal swings V_A and V_N are specified as driven into the standard load of 54.54 Ω.
- A target in the middle of a backplane drives into a load of Zbackplane / 2, which can vary from 85 / 2 = 42.5 Ω to 135 / 2 = 67.5 Ω
- For current mode drivers, the ratio of source bus swing to standard load swing is: (Zbackplane / 2) / 54.54
- Maximum ratio of Vbp / Vstd is: 1.24 = 67.5 / 54.54
- Minimum ratio of Vbp / Vstd is: 0.78 = 42.5 / 54.54

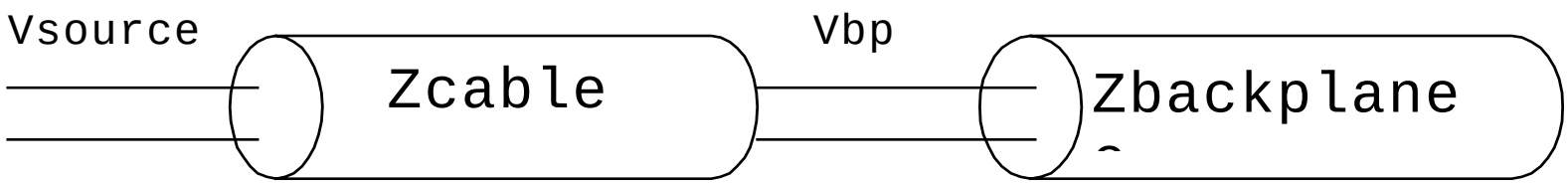
Quantum™

HBA Output Swing Into Cable

- A typical host bus adapter is located at one end of a SCSI bus
- Such an HBA will typically drive a local terminator with a resistance of 100 to 110 Ω in parallel with a cable impedance of 110 to135 Ω.
- Source signal swing relative to a standard load is the ratio of the “local terminator resistance in parallel with the cable impedance” to the standard load resistance of 54.54 Ω.
- Maximum ratio is 1.11 = (110 in parallel with 135) / 54.54
- Minimum ratio is 0.96 = (100 in parallel with 110) / 54.54

Cable Signal Into Backplane

- Cable impedance range 110 to 135 Ω
- Backplane impedance range from 85 to 135 Ω
- Ratio of the backplane amplitude to the cable amplitude is 2 * Zbp / (Zbp + Zcable)
- Maximum ratio is 1.10 = 2 * 135 / (135 + 110)
- Minimum ratio is 0.81 = 2 * 85 / (85 + 135)



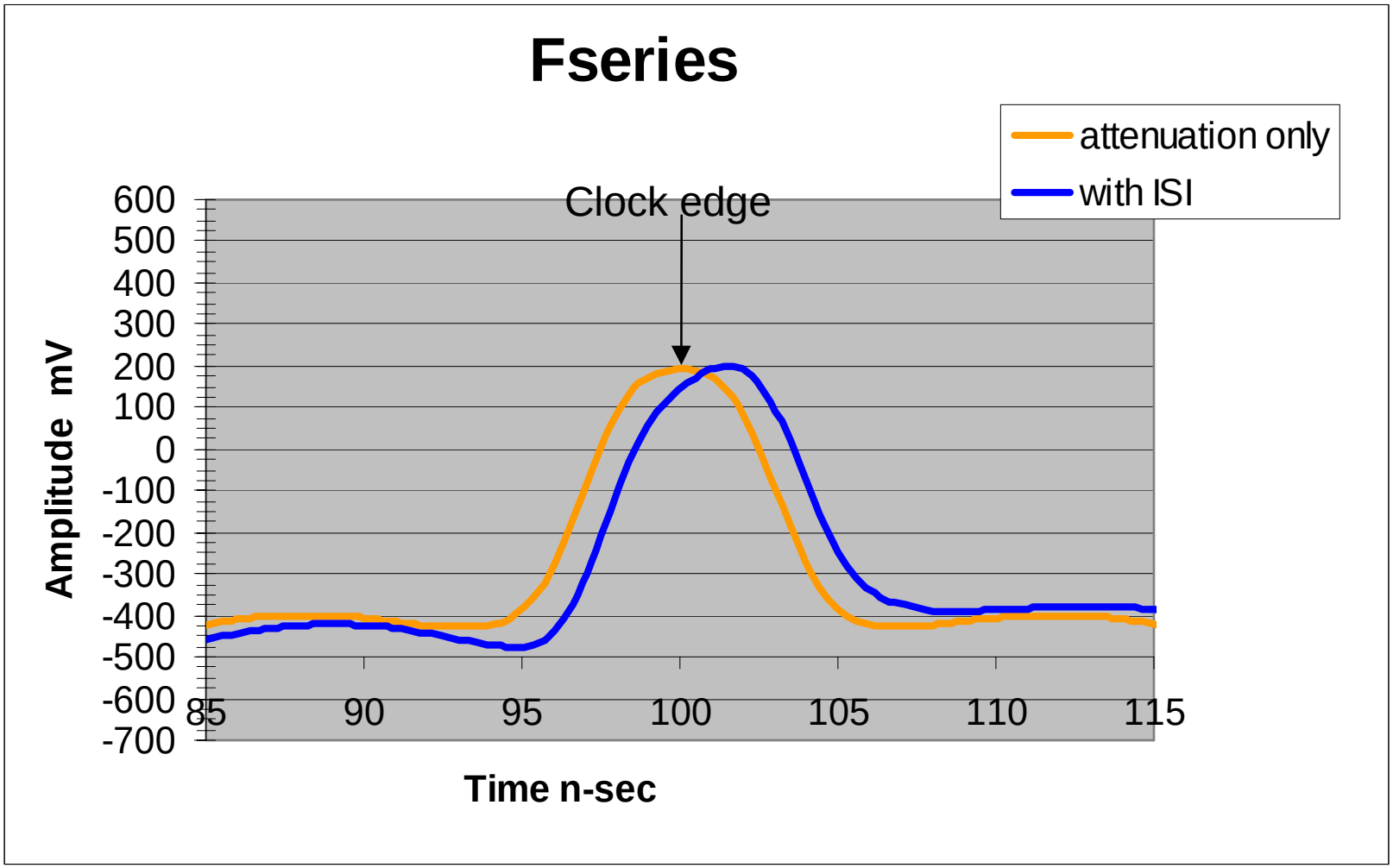
Vbp = Vsource * 2*Zbp /(Zbp + Zcable)

Voltage Ratio Equations

- HBA load is the local terminator in parallel with Zcable
- Z@drvr = (Zterm_near * Zcable) / (Zterm_near + Zcable)
- Vcable / Vstd = Z@drvr / 54.54
- Vbp / Vcable = 2 * Zbp / (Zbp + Zcable)
- Vbp = Vstd * (Vcable / Vstd) * (Fbus_loss) * (Vbp / Vcable)
- Maximum ratio is 1.11 * Fbus_loss = ((110 // 110) / 54.54) * Fbus_loss * (2 * 135 / (135 + 110)) based on:
  - Rterm_near = 110
  - Zcable = 110
  - Zbp = 135
- Minimum ratio is 0.82 * Fbus_loss = ((100 // 135) / 54.54) * Fbus_loss * (2 * 85 / (85 + 135)) based on:
  - Rterm_near = 100
  - Zcable = 135
  - Zbp = 85

ISI Shifts The Peak

- ISI (group delay dispersion) shifts the peak of the pulse away from the cell center.
- Clock edge is defined by free running clock without ISI



Summary

- D.C. losses
  - +18 / -18 mV offset variation from differences in terminator V, R from ideal load circuit.
  - +0 / -30 mV offset variation from bus resistance effects
  - Excludes the variations allowed in figure A.2 for driver balance
- A.C losses
  - The ratio of signal on a backplane to that on the specified ideal load can range from 0.82 to 1.11
  - Includes variations in terminator, cable impedance, and backplane impedance.
  - Does not include attenuation or ISI effects

Conclusions

- D.C. losses are a function of terminator characteristics and bus resistance. They are not a fraction of the signal strength.
- Only some of the D.C. errors are covered by the wedge in figure A.2.
- Analyses presented to date for Ultra320 noise margins do not include reflection losses at bus impedance discontinuities.
- Pulse shift distortion caused by ISI causes the data to be latched prior to the peak of the pulse.
- These losses and errors need to be accounted for in any accurate noise margin analysis for Ultra320 SCSI.