Date: Aug 22, 2000

To: T10 Committee (SCSI)

From: George Penokie (IBM)

Subject: Getting training started in SPI-4

Overview

The July SPI-4 working group accepted in principle that there were some problems with the timings associated with the indication of the start of a training pattern. The following shows the proposed corrections to this problem.

0.0.0.0.1 DT DATA IN phase training pattern

The target shall indicate a training pattern is going to occur on a DT DATA IN phase by:

1) negating the SEL signal a minimum of two system deskew delays before changing the MSG, C/D, and I/O signals, and
2) asserting the SEL signal a minimum of two system deskew delays and a maximum of four deskew delays after asserting the MSG and I/O signals and negating the C/D.

Editors Note 1 - GOP: The above set a maximum on how long the target can wait before it asserts SEL.

The target shall begin the A section of the training pattern no sooner than ~~two system deskew delays~~ one data release delay plus one bus settle delay after asserting the ~~SEL~~ I/O signal. The target shall transmit the following training pattern:

Editors Note 2 - GOP: The above change is need because there is a requirement that the target cannot drive the bus until 800ns after asserting the I/O signal (see section 10.13)

Start of A section;

1) disable precompensation;
2) simultaneously assert REQ, P1, and DB(15-0,P_CRCA) signals;
3) wait 32 transfer periods (e.g., 200 ns at fast-160);
4) simultaneously negate REQ, P1, and DB(15-0,P_CRCA) signals;
5) wait 32 transfer periods;
6) set precompensation to negotiated state;
7) negate SEL signal;
8) simultaneously assert and negate REQ, P1, and DB(15-0,P_CRCA) signals at the negotiated transfer period for 128 transfer periods, (e.g., 800 ns at fast-160);

Start of B section;

9) on the 128th transfer period negate P1, and DB(15-0,P_CRCA) signals while continuing to assert and negate REQ at the negotiated transfer period for 8 transfer periods (e.g., 50 ns at fast-160);
10) negate REQ for 8 transfer periods;
11) simultaneously assert and negate P1 and DB(15-0,P_CRCA) signals at twice the negotiated transfer period for while asserting and negating REQ at the negotiated transfer period for 48 transfer periods (i.e., simultaneously repeat a 1100b bit pattern 12 times on each signal);

Start of C section;

12) assert and negate REQ at the negotiated transfer period for 128 transfer periods and assert and negate P1 at twice the negotiated transfer period while repeating a 0000010011111011b bit pattern

eight times on DB(15-0,P_CRCA); and
13) After ACK negated for greater than 100ns training pattern ends.

The initiator shall begin the training pattern ~~on detection of~~ if it detects the ~~assertion of the~~ SEL, ~~signal with~~ MSG, and I/O true and C/D false on the first assertion of the REQ signal. The initiator shall transmit the following training pattern:

Editors Note 3 - GOP: The above defines at what point the initiator decides whether to do a training pattern or not. This method adds no extra overhead to the normal start of a data phase.

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1) assert ACK signal;
2) wait 32 transfer periods (e.g., 200 ns at fast-160);
3) negate ACK signal;
4) wait 32 transfer periods (e.g., 200 ns at fast-160); and
5) assert and negate ACK signal at the negotiated transfer period for 64 transfer periods, (e.g., 400 ns at fast-160).

At the completion of the training pattern the target continues asserting and negating the REQ signal at the negotiated transfer period (e.g., 6,25 ns transfer period at fast-160) and the P1 signal at twice the negotiated transfer period (e.g., 12 ns transfer period at fast-160). When the target is ready to transfer data it shall reverse the phase of P1 (see 10.8.4.3).

0.0.0.0.2 DT DATA OUT phase training pattern

The target shall request a training pattern on a DT DATA OUT phase by:

1) negating the SEL signal a minimum of two system deskew delays before changing the MSG, C/D, and I/O signals, and
2) asserting the SEL signal a minimum of two system deskew delays and a maximum of four deskew delays after asserting the MSG signal and negating the C/D and I/O signals.

Editors Note 4 - GOP: The above set a maximum on how long the target can wait before it asserts SEL.

The target shall begin the training pattern no sooner than two system deskew delays after asserting the SEL signal. The target shall transmit the following training pattern:

Editors Note 5 - GOP: There was a comment that the target should wait longer than 2 deskew delays before driving P_CRCA because the initiator my have been driving it. However, this is not the case because the target always is driving P_CRCA.

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1) disable precompensation;
2) assert REQ and P_CRCA signals;
3) wait 32 transfer periods (e.g., 200 ns at fast-160);
4) negate REQ and P_CRCA signals;
5) wait 32 transfer periods (e.g., 200 ns at fast-160);
6) set precompensation to negotiated state;
7) negate SEL signal;
8) simultaneously assert and negate REQ and P_CRCA signals at the negotiated transfer period for 64 transfer periods, (e.g., 400 ns at fast-160);

9) negate REQ and P_CRCA for a minimum of 16 transfer periods; and
10) the target shall begin asserting and negating REQ to indicate to the initiator valid data may be sent. The number of REQ transitions shall not exceed the negotiated offset.

The initiator shall begin the A section of the training pattern ~~on detection of~~ if it detects the ~~assertion of the~~ SEL and ~~signal with~~ MSG true, and C/D and I/O false on the first assertion of the REQ signal. The initiator shall transmit the following training pattern:

Editors Note 6 - GOP: The above defines at what point the initiator decides whether to do a training pattern or not. This method adds no extra overhead to the normal start of a data phase.

Start of A section;
1) simultaneously assert ACK, P1, and DB(15-0) signals;
2) wait 32 transfer periods (e.g., 200 ns at fast-160);
3) simultaneously negate ACK, P1, and DB(15-0) signals;
4) wait 32 transfer periods;
5) simultaneously assert and negate ACK, P1, and DB(15-0) signals at the negotiated transfer period for 128 transfer periods, (e.g., 800 ns at fast-160);

Start of B section;
6) on the 128th transfer period negate P1, and DB(15-0) signals while continuing to assert and negate ACK at the negotiated transfer period for 8 transfer periods (e.g., 50 ns at fast-160);
7) negate ACK for 8 transfer periods;
8) simultaneously assert and negate P1 and DB(15-0) signals at twice the negotiated transfer period for while asserting and negating ACK at the negotiated transfer period for 48 transfer periods (i.e., simultaneously repeat a 1100b bit pattern 12 times on each signal); and

Start of C section;
9) assert and negate ACK at the negotiated transfer period for 128 transfer periods and assert and negate P1 at twice the negotiated transfer period while repeating a 0000010011111011b bit pattern eight times on DB(15-0).

At the completion of the training pattern the initiator continues asserting and negating the ACK signal at the negotiated transfer period (e.g., 6,25 ns transfer period at fast-160) and the P1 signal at twice the negotiated transfer period (e.g., 12 ns transfer period at fast-160). When the initiator is ready to transfer data and there are outstanding REQs it shall reverse the phase of P1 (see 10.8.4.3).