T10/00-323r3

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John Lohmeyer
T10 Chairman

Subject: **Proposal for revision of the timing tables and definitions in SPI-4**

This proposal utilizes the timing budget already accepted into SPI-4 and completes the homework to use the timing budget as the basis for modifying the related timing tables, definitions, and figures. Revision two is the result of the working group meeting on 8/24/2000.

The working group selected alternative one from revision one of the proposal. This is the alternative that documents the observable timing as it would appear with an oscilloscope. Closure has not been reached on the ATN timing and Bill Galloway took an action item to analyze ATN in the environment of a free running ACK and to bring in a proposal for any needed additional change for ATN. Revision 3 adds to note 1 on page 13 of 13 "transmitter chip skew" that was inadvertently omitted from the note in Revision 2.

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p.s. Clause numbers, figure numbers, and table numbers are as FrameMaker determined and have not been synchronized exactly to SPI-4. Some bolding is on purpose and some is a fluke of FrameMaker. Correcting these format differences could be fun and games for the SPI-4 technical editor. Since time to wrestle with FrameMaker was finite, some figure cleanup was left also for editor amusement.

9 SCSI parallel bus timing

9.1 SCSI parallel bus timing values

See table 30, and table 31 for SCSI bus timing values. Unless otherwise indicated, the ~~delay~~ time measurements for each SCSI device, shown in table 30, shall be calculated from signal conditions existing at that SCSI device's port. The timing characteristics of each signal are described in the following paragraphs. Timing requirements relating to LVD release glitches are defined in 7.3.4.1.

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Table 28 - SCSI bus data & information phase DT timing values

Sub-clause	Timing description	Type	Timing Values (note 4)(note 7)(note 8)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
9.2.2	**ATN transmit setup time**	min	48,4 ns	29,2 ns	19,6 ns	14,8 ns	11,675 ns
9.2.3	**ATN receive setup time**	min	13,6 ns	7,8 ns	4,9 ns	3,45 ns	4,825 ns
9.2.8	Cable skew (note 1)	max	4 ns	3 ns	2,5 ns	2,5 ns	2,5 ns
9.2.9	pCRC receive hold time	min	11,6 ns	5,8 ns	2,9 ns	1,45 ns	N/A
9.2.10	pCRC receive setup time	min	18,6 ns	12,8 ns	9,9 ns	8,45 ns	N/A
9.2.11	pCRC transmit hold time	min	38,4 ns	19,2 ns	9,6 ns	4,8 ns	N/A
9.2.12	pCRC transmit setup time	min	48,4 ns	29,2 ns	19,6 ns	14,8 ns	N/A
9.2.21	Receive assertion period (note 2)	min	80 ns	40 ns	20 ns	8,5 ns	4,74 ns
9.2.22	Receive hold time (note 2 and note 3)	min	11,6 ns	5,8 ns	2,9 ns	1,45 ns	(0,08) ns
9.2.23	Receive negation period (note 2)	min	80 ns	40 ns	20 ns	8,5 ns	4,74 ns
9.2.24	Receive setup time (note 2 and note 3)	min	11,6 ns	5,8 ns	2,9 ns	1,45 ns	(6,33) ns
9.2.25	Receive REQ (ACK) period tolerance	min	0,7 ns	0,7 ns	0,7 ns	0,7 ns	0,06 ns
9.2.26	Receive REQ assertion period with P_CRCA transitioning	min	85,5 ns	48 ns	32,5 ns	21 ns	N/A
9.2.27	Receive REQ negation period with P_CRCA transitioning	min	85,5 ns	48 ns	32,5 ns	21 ns	N/A
9.2.34	Signal timing skew	max	26,8 ns	13,4 ns	6,7 ns	3,35 ns	4,85 ns
9.2.28	REQ (ACK) period	**nom**	200 ns	100 ns	50 ns	25 ns	12,5 ns
9.2.36	Transmit assertion period (note 2)	min	92 ns	46 ns	23 ns	11,5 ns	5,69 ns
9.2.37	Transmit hold time (note 2 and note 3)	min	38,4 ns	19,2 ns	9,6 ns	4,8 ns	4,77 ns
9.2.38	Transmit negation period (note 2)	min	92 ns	46 ns	23 ns	11,5 ns	5,69 ns
9.2.39	Transmit setup time (note 2 and note 3)	min	38,4 ns	19,2 ns	9,6 ns	4,8 ns	(1,48) ns
9.2.40	Transmit REQ (ACK) period tolerance	max	0,6 ns	0,6 ns	0,6 ns	0,6 ns	0,06 ns

Notes:

1 Cable skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.

2 See 9.3 for measurement points for the timing specifications.

3 See 9.4 for examples of how to calculate setup and hold timing.

4 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.

5 Fast =<80 times calculated without the benefit of ISI compensation. For Fast 160 ISI compensation is assumed to eliminate 50% of the time shift due to ISI.

6 Calculated with the benefit of ISI compensation and skew compensation.

7 Setup and hold times are 1,0 ns better if ISI compensation is invoked for Fast 160.

8 Fast 160 SCSI devices shall not change timing parameters between training events or reset events.

Table 28 - SCSI bus data & information phase DT timing values

Sub-clause	Timing description	Type	Timing Values (note 4)(note 7)(note 8)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
9.2.41	Transmit REQ assertion period with P_CRCA transitioning	min	97,5 ns	54 ns	35,5 ns	24 ns	N/A
9.2.42	Transmit REQ negation period with P_CRCA transitioning	min	97,5 ns	54 ns	35,5 ns	24 ns	N/A
	Transmit ISI Compensation	max	Note 5	Note 5	Note 5	Note 5	1,0 ns
	Receive Skew Compensation	max	N/A	N/A	N/A	N/A	4,4 ns
	Residual Skew Error	max	49 ns	24 ns	11,5 ns	5,25 ns	± 0,15 ns
	Strobe Offset Tolerance	max	N/A	N/A	N/A	N/A	± 0,125 ns
	Net Receive Internal Setup/Hold Time (note 6)	min	0,5 ns	0,5 ns	0,5 ns	0 ns to 1,95 ns	0,345 ns

Notes:
1 Cable skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.
2 See 9.3 for measurement points for the timing specifications.
3 See 9.4 for examples of how to calculate setup and hold timing.
4 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.
5 Fast =<80 times calculated without the benefit of ISI compensation. For Fast 160 ISI compensation is assumed to eliminate 50% of the time shift due to ISI.
6 Calculated with the benefit of ISI compensation and skew compensation.
7 Setup and hold times are 1,0 ns better if ISI compensation is invoked for Fast 160.
8 Fast 160 SCSI devices shall not change timing parameters between training events or reset events.

Table 29: SCSI Fast-160 Timing Budget Template

Item	Fast-160	Comments
Nominals:		
REQ(ACK) Period	**12,5 ns**	
Data transfer period	**6,25 ns**	
Ideal Setup/Hold	**3,125 ns**	
Non-compensatable:	**Early to Late**	**Worse case total of + and - time shift unless otherwise noted**
REQ(ACK) period tolerance / 2	**0,06 ns**	**Tolerance of transmitter plus measurement error Note 1**
Driver time asymmetry	**0,50 ns**	
Receiver time asymmetry	**0,35 ns**	
System noise at launch	**0,25 ns**	**Time impact**

Table 29: SCSI Fast-160 Timing Budget Template

Item	Fast-160	Comments
System noise at receiver	**0,25 ns**	**Time impact**
~~Near end~~ Crosstalk	**0,7 ns**	**Time impact**
Chip noise in receiver	**0,2 ns**	**Time impact**
Receiver amplitude time skew	**0,2 ns**	**With minimum signals**
Clock jitter	**0,25 ns**	
Strobe offset tolerance	**0,5 ns**	**Accuracy of centering strobe**
Residual Skew error	**0,3 ns**	**After skew compensation**
Non-compensatable total:	**3,56 ns**	
Compensatable skew:		**Worse case**
Transmitter chip skew	**0,75 ns**	
Receiver chip skew	**0,75 ns**	
Cable skew	**2,5 ns**	
Two x trace skew	**0,4 ns**	**Total for SCSI device pair**
ISI of data	**4,0 ns**	**Worse case pattern measured (+2 ns/ -1 ns)**
ISI of REQ(ACK)	**0,0 ns**	**Post preamble**
May detect to shall detect ambiguity	**0,0 ns**	**Assumed to be negligible in given chip**
Compensatable total:	**8,4 ns**	
ISI Compensation	**2,0 ns**	**(+1ns / -0,5 ns)**
Skew compensation	**4,4 ns**	
Compensation total:	**6,4 ns**	
Total Error Inputs:	**11,96 ns**	
Post compensation error:	**5,56 ns**	
Minimum data valid window (data time-net error)	**0,69 ns**	**Note 2, Note 3**

Notes:
1) Tolerance adjusted for half cycle (data transfer period)
2) Fast-80 budget in SPI-3 neglects asymmetry & detection ambiguity and lumps chip noise, clock jitter, crosstalk, noise, ISI and receiver amplitude skew into other terms (e.g., signal distortion skew) and/or ignores the effects.
3) Minimum compensated setup and hold half this value.

9.2 Timing description

9.2.2 ATN transmit setup time

The minimum time provided by the transmitter between the assertion of the ATN signal and the negation of the last ACK signal. Specified to provide the increased ATN receive setup time, subject to intersymbol interference, cable skew, and other distortions.

9.2.3 ATN receive setup time

The minimum time required at the receiver between the assertion of the ATN signal and the negation of the ACK signal to recognize the assertion of an Attention Condition. Specified to ease receiver timing requirements.

NOTE 24 - ~~Previous~~ Versions of this standard prior to SPI-3 provided two system deskew delays of setup time.

9.2.8 Cable skew

The maximum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices excluding any signal distortion skew delays.

TBD **Chip noise in receiver**

The maximum ~~intrinsic short term~~ transition to transition time shift due to the internal physics of the receiving SCSI device circuitry.

TBD **Clock jitter**

The maximum ~~short term~~ transition to transition time shift of SCSI bus signals caused by short term variations in the transmitting SCSI device's clock ~~logic~~.

TBD Net receive internal setup and hold times

The minimum times provided for setup or hold time in the receive data detector after allowance for timing errors and timing compensation from all sources.

9.2.9 pCRC receive hold time

The minimum time required at the receiver between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled (see 16.3.10).

9.2.10 pCRC receive setup time

The minimum time required at the receiver between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled (see 16.3.10). Specified to ease receiver timing requirements and ensure that this signal, which is outside CRC protection, is received correctly.

9.2.11 pCRC transmit hold time

The minimum time provided by the transmitter between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled (see 16.3.10).

9.2.12 pCRC transmit setup time

The minimum time provided by the transmitter between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled (see 16.3.10). Specified to provide the increased receive setup time, subject to intersymbol interference, cable skew, and other distortions. For Fast 160 this time is not applicable. Editor's note: When Fast 160 data groups are restored to the standard this time is the same as transmit setup time.

9.2.15 Net Receive Internal Setup and Hold times

The net effective setup or hold time measured within the receiving SCSI device from the worse case bit (data or parity) to the compensated offset strobe. This time may not be observable to other than the SCSI

device designer. Failure to meet the requirement may only be observable in terms of increased error rates.

9.2.21 Receive assertion period

The minimum time ~~required~~ provided at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers, for =< Fast 80 provided P_CRCA is not transitioning with pCRC protection enabled (see 16.3.10). Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 0,8 V level. For SE fast-20 operation the period is measured at the 1,0 V level. For LVD see figure 46 and figure 47 for signal measurement points.

Editor's note: I still think all the extra detail added to this definition is out of place and not needed.

9.2.22 Receive hold time

For ST data transfers the minimum time ~~required~~ provided at the receiving SCSI device between the assertion of the REQ signal or the ACK signals and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled (see 16.3.10). For DT data transfers the minimum time required at the receiving SCSI device between the transition (i.e. assertion or negation) of the REQ signal or the ACK signals and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous data transfers.

~~NOTE 19 - This definition may need to be tweaked depending upon the final method chosen in the timing tables to show the results of the timing budget.~~

9.2.23 Receive negation period

The minimum time ~~required~~ provided at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous data transfers. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 2,0 V level. For SE fast-20 operation the period is measured at the 1,9 V level. For LVD see figure 46 and figure 47 for signal measurement points.

9.2.24 Receive setup time

For ST data transfers the minimum time ~~required~~ provided at the receiving SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the assertion of the REQ signal or the ACK signal while using synchronous data transfers. For DT data transfers the minimum time required at the receiving SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the transition of the REQ signal or the ACK signal while using synchronous data transfers.

~~NOTE 20 - This definition may need to be tweaked depending upon the final method chosen in the timing tables to show the results of the timing budget.~~

9.2.25 Receive REQ (ACK) period tolerance

The minimum tolerance that a SCSI device shall allow to be subtracted from the REQ (ACK) period. The tolerance comprises the transmit REQ (ACK) tolerance plus a measurement error due to noise.

9.2.26 Receive REQ assertion period with P_CRCA transitioning

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers with P_CRCA transitioning with pCRC protection enabled (see 16.3.10). Specified to ensure that the assertion period is longer than the receive hold time plus the receive setup time. For Fast 160 this time is not applicable. Editor's note: When Fast 160 data groups are restored to the standard this time is the same as transmit setup time.

9.2.27 Receive REQ negation period with P_CRCA transitioning

The minimum time required at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous data transfers with P_CRCA transitioning with pCRC protection enabled (see 16.3.10). Specified to ensure that the negation period is longer than the receive hold time plus the receive setup time. For Fast 160 this time is not applicable. Editor's note: When Fast 160 data groups are restored to the standard this time is the same as transmit setup time.

9.2.29 Receive Skew Compensation

The effective reduction in worse case timing skew of data, parity, and strobe signals provided by the receiving SCSI device but not directly observable at the receiving SCSI device connector.

TBD Receiver amplitude time skew

The maximum time shift of SCSI bus signals caused by the difference in receiver switching delay of a minimum amplitude signal versus a maximum amplitude signal.

9.2.28 REQ (ACK) period

The REQ (ACK) period during synchronous data transfers, specified in table 30 for ST DATA phases and in table 31 for DT DATA phases, is the nominal time between adjacent assertion edges of the REQ or ACK signal for the fastest negotiated data transfer rate. For the purpose of calculating the actual REQ (ACK) period tolerance the REQ (ACK) period should be measured without interruptions (e.g., offsets pauses). To
minimize the impact of crosstalk and ISI the measurements should be made by averaging the time between edges during long (i.e., greater than 512 bytes) all zero or all ones data transfers and by ignoring the first and last 10 transitions.

In DT DATA phases the negotiated transfer period for data is half of the REQ (ACK) period since data is qualified on both the assertion and negation edges of the REQ or ACK signal. In ST DATA phases the negotiated transfer period for data is equal to the REQ (ACK) period during synchronous data transfers since data is only qualified on the assertion edge of the REQ or ACK signal.

TBD Residual skew error

The maximum timing error between the deskewed data and REQ or ACK internal to the receiving SCSI device after skew compensation.

9.2.34 Signal timing skew

The maximum signal timing skew occurs when transferring random data and, for =< Fast 80, in combination with interruptions of the REQ or ACK signal transitions (e.g., pauses caused by offsets). The signal timing skew includes cable skew (measured with 0101... patterns) and signal distortion skew caused by random data patterns and transmission line reflections as shown in figure 44, figure 45, figure 46, and figure 47. The receiver detection range is the part of the signal between the "may detect" level and the "shall detect" level on either edge. (see 9.3)

NOTE 21 - For timing budget purposes the value stated in the tables XX is calculated without the benefit of skew compensation.

TBD **System noise at launch**

The maximum time shift of SCSI bus signals caused by system noise at the transmitter (e.g., noise caused by current changes in the voice coil) measured at the transmitting SCSI device connector.

TBD **System noise at receiver**

The maximum time shift of SCSI bus signals caused by system noise at the receiver (e.g., noise caused by current changes in the voice coil) measured at the receiving SCSI device connector not including the time shift from the system noise at launch.

9.2.37 Strobe offset tolerance

~~The tolerance on the time used to delay the compensated REQ/ACK to strobe the data and parity signals provided by the receiving SCSI device but not directly observable at the receiving SCSI device connector.~~ The time tolerance of centering the compensated REQ or ACK strobe in the transfer period during the training pattern.

TBD Time asymmetry

The maximum time difference between the asserted and negated signal for ~~alternating states~~ data, REQ, or ACK transitions that are intended to ~~have equal times~~ be equidistant.

9.2.36 Transmit assertion period

The minimum time that a target shall assert the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled (see 16.3.10). Also, the minimum time that an initiator shall assert the ACK signal while using synchronous data transfers.

9.2.37 Transmit hold time

For ST data transfers the minimum time provided by the transmitting SCSI device between the assertion of the REQ signal or the ACK signal and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous data transfers. For DT data transfers the minimum time provided by the transmitting SCSI device between the transition of the REQ signal or the ACK signal and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous data transfers.

~~NOTE 22 - This definition may need to be tweaked depending upon the final method chosen in the timing tables to show the results of the timing budget.~~

9.2.41 Transmit ISI Precompensation

The effective reduction in worse case ISI timing shift provided by the transmitting SCSI device as seen at the receiving SCSI device connector.

9.2.38 Transmit negation period

The minimum time that a target shall negate the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled (see 16.3.10). Also, the minimum time that an initiator shall negate the ACK signal while using synchronous data transfers.

9.2.39 Transmit setup time

For ST data transfers the minimum time provided by the transmitting SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the assertion of the REQ signal or the ACK signal while using synchronous data transfers. For DT data transfers the minimum time provided by the transmitting SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the transition of the REQ signal or the ACK signal while using synchronous data transfers.

~~NOTE 23 - This definition may need to be tweaked depending upon the final method chosen in the timing tables to show the results of the timing budget.~~

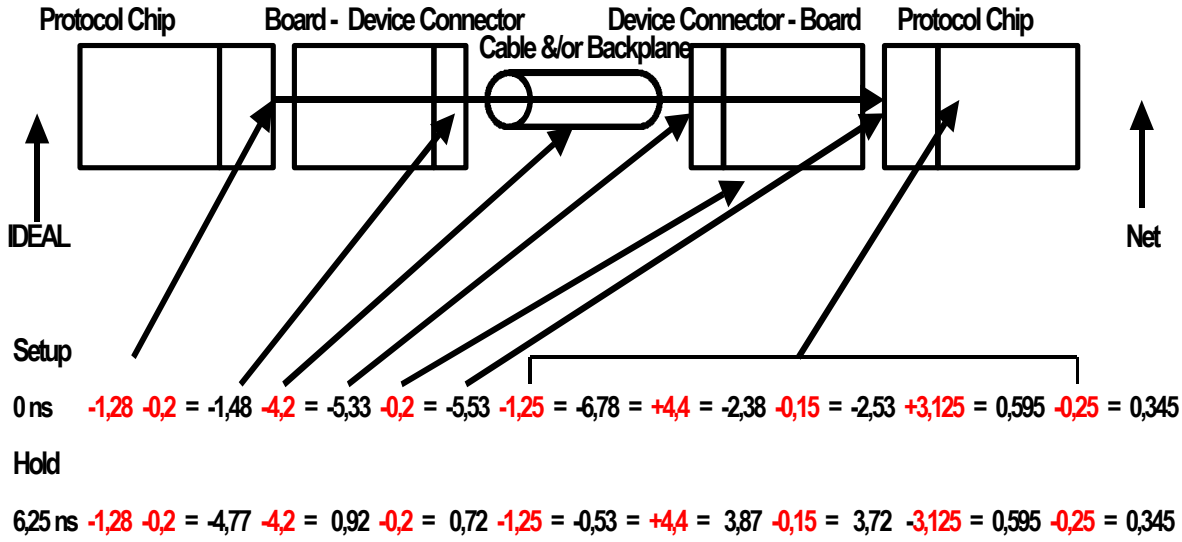
9.2.40 Transmit REQ (ACK) period tolerance

The maximum tolerance that a SCSI device may subtract from the REQ (ACK) period.

9.2.41 Transmit REQ assertion period with P_CRCA transitioning

The minimum time that a target shall assert the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled (see 16.3.10). Specified to provide the increased receive REQ assertion period, subject to loss on the interconnect. For Fast 160 this time is not applicable. Editor's note: When Fast 160 data groups are restored to the standard this time is the same as transmit setup time.

Application of timing budget - skew block diagram with pre-compensation



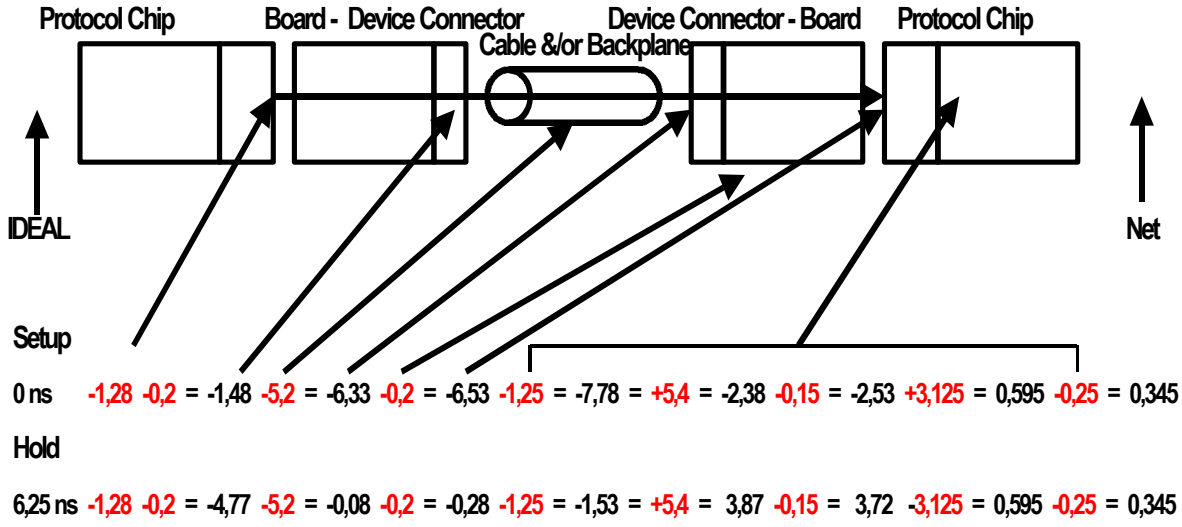
Notes:

1) The transmitting SCSI device may reduce or increase the timing margin by the following worse case factors: bit period tolerance (i.e., REQ(ACK) Period Tolerance / 2); driver asymmetry; clock jitter; system noise at launch; pre-compensation; and board skew.

2) The transmission of data from one SCSI device to another may have the timing margin reduced by the signal timing skew that comprises the following worse case factors; crosstalk; cable skew; and ISI. If precompensation is invoked the worse case signal timing skew is reduced by the ISI compensation value. Portions of the crosstalk and ISI may also be observable at the transmitting device connector. Consequently transmit setup and transmit hold time should be measured with an alternating pattern at the negotiated data rate with all data signals other than that being measured held at a continual assertion or negation.

3) The reception of data within a SCSI device may have the timing margin reduced or increased by the following additional worse case factors: board skew; receiver amplitude time skew; receiver chip skew; receiver time asymmetry; system noise at the receiver; receiver chip noise (applied at receiver due to small signal physics); ISI compensation; skew compensation; strobe offset tolerance; and residual skew error.

Application of timing budget - skew block diagram with post-compensation



Notes:

1) The transmitting SCSI device may reduce the timing margin by the following worse case factors: bit period tolerance (i.e., REQ(ACK) Period Tolerance / 2); driver asymmetry; transmitter chip skew, clock jitter; system noise at launch; and board skew.

2) The transmission of data from one SCSI device to another may have the timing margin reduced by the signal timing skew that comprises the following worse case factors; crosstalk; cable skew; and ISI. If precompensation is invoked the worse case signal timing skew is reduced by the ISI compensation value. Portions of the crosstalk and ISI may also be observable at the transmitting device connector. Consequently transmit setup and transmit hold time should be measured with an alternating pattern at the negotiated data rate with all data signals other than that being measured held at a continual assertion or negation.

3) The reception of data within a SCSI device may have the timing margin reduced or increased by the following additional worse case factors: board skew; receiver amplitude time skew; receiver chip skew; receiver time asymmetry; system noise at the receiver; receiver chip noise (applied at receiver due to small signal physics); ISI compensation; skew compensation; strobe offset tolerance; and residual skew error.