To: T-10/SPI-4 Working Group
From: Richard Moore
QLogic Corp.
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Subject: Disabling Precompensation

In Table 55 of SPI-4 rev 0, byte 7 bit 7 of the PPR message is labeled P_EN. The text states that P_EN is “precompensation enabled” and is set to zero to cause the device receiving the PPR message to disable precompensation on all signals transmitted during DT DATA phases. When set to one, the device receiving the PPR message shall enable precompensation during DT DATA phases. Additionally, the text states that P_EN shall be set to zero for negotiated transfer periods greater than 6.25 ns.

We believe this should be changed for the following reasons:

1. The normal state for devices running Fast-160 transfers is to enable precompensation. The normal state should be represented by a value of zero, and the exceptional state should be represented by a value of one.
2. The specification amounts to a prohibition against using precompensation on devices that negotiate to transfer rates slower than Fast-160.
3. If there are legacy (SPI-3) devices that implement precompensation, they are in effect broken by the P_EN requirements since they are unaware of the P_EN bit.

We propose that the following two changes be incorporated into SPI-4:

1. Change P_EN to PCMP_DIS with a definition that is opposite to the current definition of P_EN.
2. Remove the restrictions on the value of this bit for transfers slower than Fast-160.