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T10/00-319r0

LVD Driver Balance for Ultra320 SCSI

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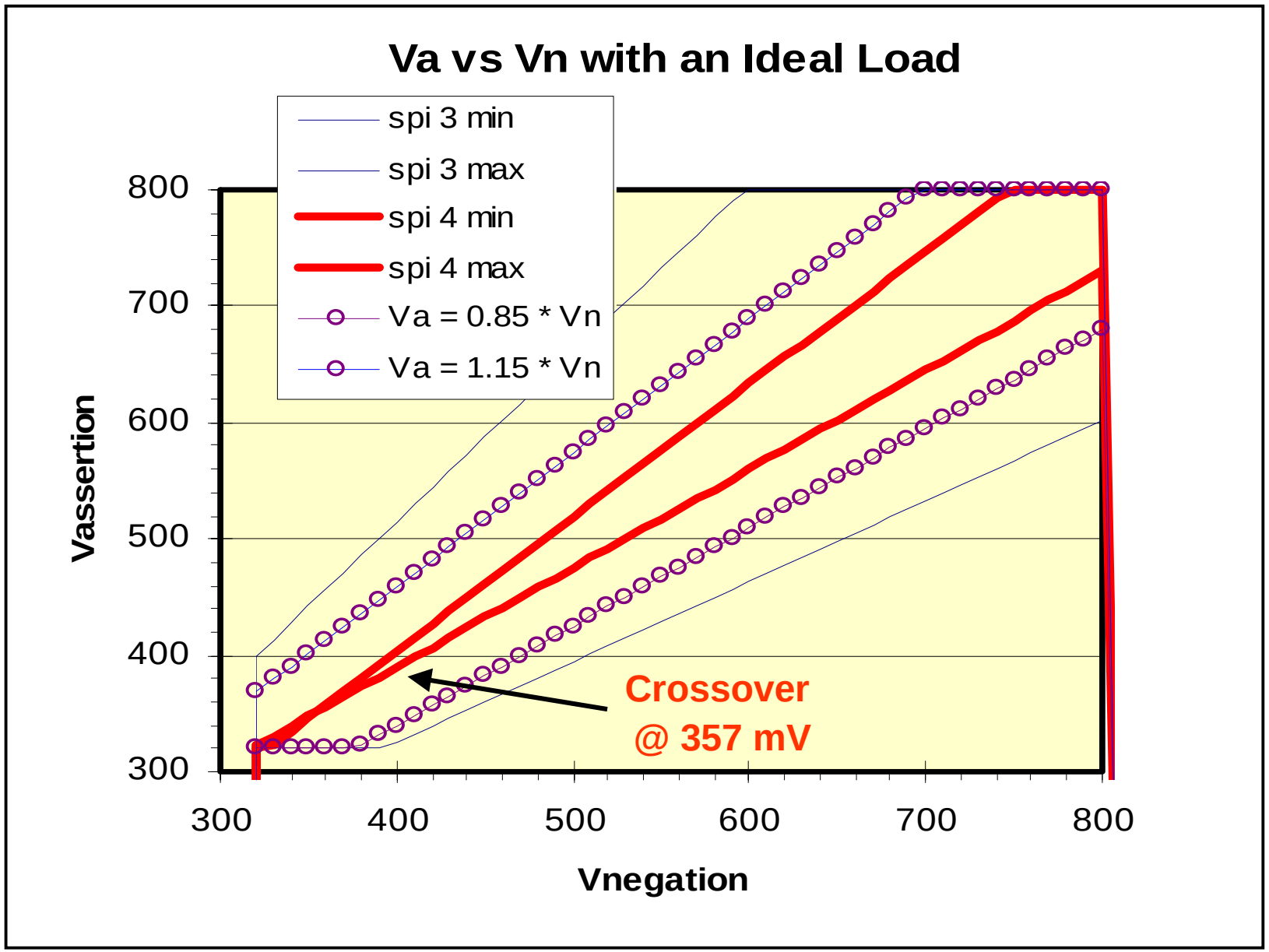
SPI-4 Table A.2 and Figure A.2

- During the July 2000 Parallel SCSI working group and subsequent plenary, the equations specifying assertion and negation D.C. levels in SPI-4 were changed in Table A.2 – Driver steady-state test limits and conditions.
- This change resulted in a decrease in the shaded area in Figure A.2 – Domain for driver assertion and negation levels.
- Closer review of these equations has raised several issues which warrant further discussion.
- In this presentation we will discuss the issues and propose an alternative set of equations that resolve those issues.

Plot of SPI Balance Equations



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SPI-2, -3, and -4 Balance Equations

- The SPI-2 and SPI-3 equations are:
  - $V_{A\_max} = 1.45 * V_N - 65$
  - $V_{A\_min} = 0.69 * V_N + 50$
- The equations voted into SPI-4 from T10/00-276r0 are:
  - $V_{A\_max} = 1.15 * V_N - 57$
  - $V_{A\_min} = 0.85 * V_N + 50$
- The result is that the lines described by the equations in SPI-4 for V_{A_max} and V_{A_min} intersect at 357 mV.
- The equations in the drawing on the last page of T10/00-276r0 are approximately:
  - $V_{A\_max} = 1.15 * V_N$
  - $V_{A\_min} = 0.85 * V_N$
  - These are not symmetrical, since 1 / 0.85 = 1.18 , 1.15

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Issues with New SPI-4 Equations

- These new SPI-4 limits apply to non-paced and non-DT operation as well, and disallow all existing LVD SCSI hardware.
- Minimum non-precomp drive strength is raised from 320 mV to 357 mV because the min and max lines cross at 357 mV.
- With the minimum cutback level set at 357 mV, the minimum full strength drive for a precompensated signal is calculated:
  - 457 mV = 357 / 0.78 for 22% cutback
  - 476 mV = 357 / 0.75 for 25% cutback
  - 535 mV = 357 / 0.67 for 33% cutback
  - 594 mV = 357 / 0.60 for 40% cutback:
- At 357 mV, there is no tolerance for the balance of V_A & V_N.
- Reasonable driver balance tolerances only exist above approximately 650 mV.

Specifying Driver Balance

- The D.C. balance max and min specs takes the form:
  $V_A = m * V_N + V_{cnc}$ where:
  - m = matching ratio between positive and negative signal currents
  - V_{cnc} = error voltage from mismatch between the bias cancellation current and the terminator negation bias current
- The slope term m represents a ratio of two IC generated currents.
- Matching IC currents to another on-chip structure is much better than trying to match IC currents to an absolute current.
- Mismatches arise from distribution of analog references, drops across the chip, thermal differences, and intra-chip component mismatches.
- Our proposed slope mismatch is 10%.

Voltage Offsets

- Matching IC currents to an absolute current (2.11 mA for the load circuit used for table A.2) is more difficult than matching on-chip currents to each other.
- In addition to the variables affecting slope, matching against an absolute current involves the generation of on-chip precision analog references and the tolerances of external components.
- Our proposed tolerance is 20%.
- Then, V_{cnc} = 23 mV = 20% * 115 mV
- So the V_A versus V_N equation would become:

$$V_{A\_min} = 0.90 * \left| V_N \right| - 23\ mV$$

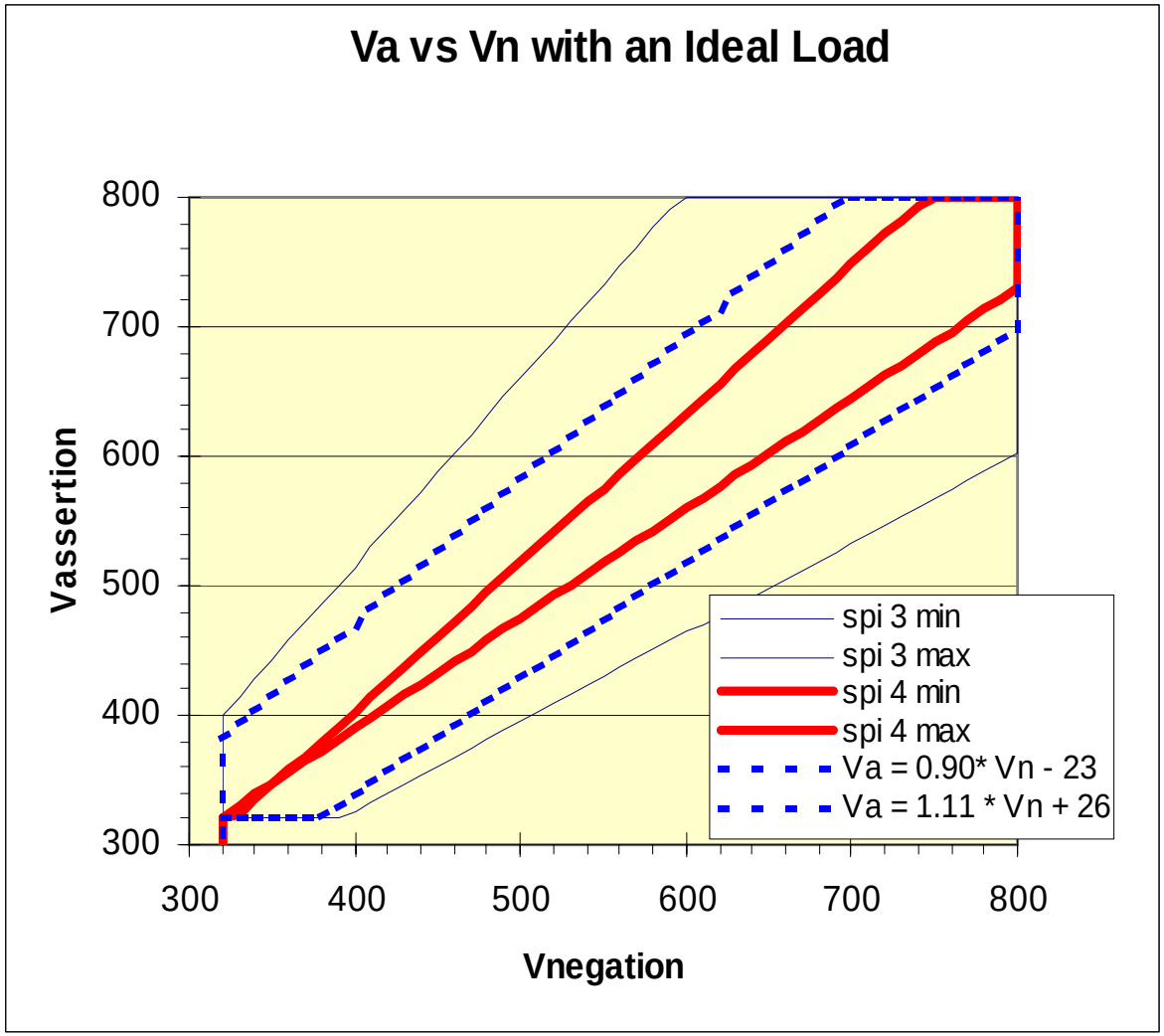
- For symmetry:

$$V_{A\_max} = 1.11 * \left| V_N \right| + 26\ mV$$

Proposed Equations vs. SPI-3 & SPI-4

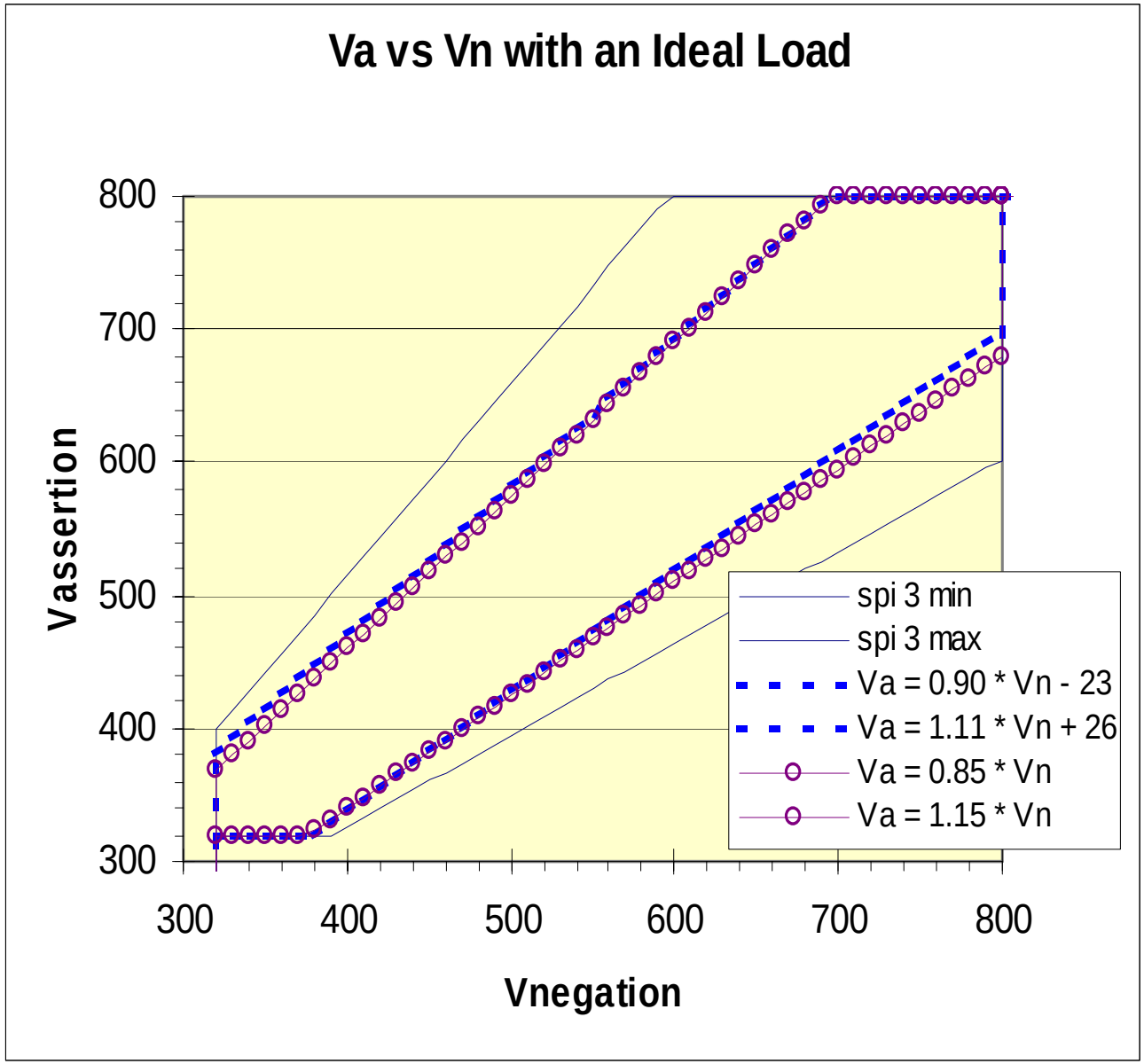
- The proposed equations provide adequate driver balance margin across the full range of drive strengths.

- SPI-4 area = 0.23 * SPI-3 area
- Proposed area = 0.62 * SPI-3 area
- Proposed maximum: $V_A = 1.11 * |V_N| + 26$
- Proposed minimum: $V_A = 0.90 * |V_N| - 23$
- SPI-4 changes required in:
  - Table A.2
  - Figure A.2



Proposal Compared to ±15% Range

- The proposed range has the same area as the +/-15% range of T10/00-276r0.
- The proposed range is more symmetrical about the line $V_A = V_N$.



Summary and Recommendations

- The SPI-4 LVD driver balance equations approved in July are very tight and disallow all existing LVD SCSI devices.
- It is recommended that the driver balance limits for SPI-4 be relaxed but remain much tighter than those in SPI-3.
- The slope of the equations of table A.2 and figure A.2 should reflect the matching of current sources within an IC.
- The offset term in the equations of table A.2 and figure A.2 should reflect the matching of an on-chip current source to an absolute current defined by the load circuit of figure A.1.
- New equations are proposed for Table A.2 in SPI-4 resulting in a wedge diagram in Figure A.2 which has an area that is 62% of the SPI-3 wedge:
  - $V_{A\_max} = 1.11 * |V_N| + 26\ mV$
  - $V_{A\_min} = 0.90 * |V_N| - 23\ mV$