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To: T10 Technical committee
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Date: 03 August 2000

Subject: Proposal for an "assertion handshaking" protocol for Ultra320 SCSI in SPI-4

Introduction

For Ultra320 paced data transfers, one signal is a free-running clock (REQ for paced DT DATA IN transfers and ACK for paced DT DATA OUT transfers). The other signal is used for flow control, incrementing (REQ) or decrementing (ACK) the current synchronous REQ/ACK offset. Since all Ultra320 transfers are information unit transfers and thus are restricted to multiples of two data transfers (32 bits), there is no need to acknowledge each data transition. The following is a proposal to use only the asserting edge of the flow control signal to acknowledge two data transitions. By using only the asserting edge of the flow control signal, the frequency of the clock required for flow control inside a device would be half that of the clock that would be required for using both edges of the signal.

The following are the specific changes required in SPI-4 to implement this proposal. The clauses in this proposal are intended to replace (or, where noted, be added) to the corresponding clauses in SPI-4. The clauses referenced are relative to the draft standard SCSI Parallel Interface – 4 (SPI-4) revision 0 available at ftp://ftp.t10.org/t10/drafts/spi4/spi4r00.pdf.

4.10 Negotiation

REQ(ACK) offset: For ST DATA transfers the REQ(ACK) offset is the number of REQ assertions that may be sent by the target in advance of the number of ACK assertions received from the initiator establishing a pacing mechanism.

For DT DATA transfers not using pacing the REQ(ACK) offset is the number of REQ transitions that may be sent by the target in advance of the number of ACK transitions received from the initiator establishing a pacing mechanism.

For paced DT DATA IN transfers the REQ(ACK) offset is the number of P1 phase enabled, data valid REQ assertions (see 10.8.4.3) that may be sent by the target in advance of ACK assertions received from the initiator, establishing a data pacing mechanism.

For paced DT DATA OUT transfers the REQ(ACK) offset is the number of REQ assertions that may be sent by the target in advance of the number of P1 phase enabled, data valid ACK assertions (see 10.8.4.3) received from the initiator, establishing a data pacing mechanism.

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10.8.4.1 Paced transfer overview

Paced transfer is optional and is only used in DT DATA phases. If a paced transfer agreement has been established it shall be used in DT DATA phases. If a paced transfer agreement has been established information unit transfers shall be used. The agreement also specifies the REQ/ACK offset and the transfer period (see 16.3.10).

When paced transfers are being used data shall be transferred using DT data transfers on 16-bit wide buses that transmit and receive data using LVD transceivers.

During paced DT data transfers, if the phase of the P1 signal indicates data is valid (see 10.8.4.3) on REQ or ACK assertions, data shall be clocked by the originating SCSI device by both the assertion and negation of the REQ or ACK signal lines. The receiving SCSI device shall clock DT data on both the assertion and negation of the REQ or ACK signal line after having been processed by the receiving SCSI device. If the phase of the P1 signal indicates data is invalid on REQ or ACK assertions, data shall not be clocked by the originating SCSI device and shall be ignored by the receiving SCSI device.

If driver precompensation is enabled at the originating SCSI device, the originating SCSI device shall apply driver precompensation to all the data, parity, REQ, and ACK signals.

For paced DT DATA IN phases the REQ/ACK offset specifies the maximum number of P1 phase enabled, data valid REQ assertions that shall be sent by the target in advance of the number of ACK assertions received from the initiator. If the number of P1 phase enabled, data valid REQ assertions exceeds the number of ACK assertions by the REQ/ACK offset, the target shall change P1 to enable the data invalid state prior to the next assertion of REQ and shall not change P1 to enable a data valid state until after the next ACK assertion is received. For successful completion of a paced DT DATA IN phase the number of P1 phase enabled, data valid REQ assertions and ACK assertions shall be equal. Each assertion indicates a single 32-bit data transfer.

For paced DT DATA OUT phases the REQ/ACK offset specifies the maximum number of REQ assertions that shall be sent by the target in advance of the number of P1 phase enabled, data valid ACK assertions received from the initiator. If the number of REQ assertions exceeds the number of P1 phase enabled, data valid ACK assertions by the REQ/ACK offset, the target shall not assert REQ until after the next P1 phase enabled, data valid ACK assertion is received. For successful completion of a paced DT DATA OUT phase the number of REQ assertions and P1 phase enabled, data valid ACK assertions shall be equal. Each assertion indicates a single 32-bit data transfer.

Implementers shall not use the following subclauses for timing requirements. For timing requirements see 9.2.

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[The following are two new paragraphs to be added below the paragraph on REQ/ACK offsets following Table 56 - TRANSFER PERIOD FACTOR field in 16.10.3.1.]

For paced DT DATA IN transfers the REQ/ACK OFFSET is the maximum number of P1 phase enabled, data valid REQ assertions allowed to be outstanding before a corresponding ACK assertion is received at the target. The width of a data transfer shall be 2 bytes. Each assertion indicates a 32-bit data transfer.

For paced DT DATA OUT transfers the REQ/ACK OFFSET is the maximum number of REQ assertions allowed to be outstanding before a corresponding P1 phase enabled, data valid ACK assertion is received at the target. The width of a data transfer shall be 2 bytes. Each assertion indicates a 32-bit data transfer.