Quantum™

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# Flow Control

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# Assertion of P_CRCA

- When P_CRCA is asserted for purposes of flow control:
  - DataIn Phase - Target shall assert P0 before the last 4 valid data or crc transfers of the last packet of the stream. "Valid data transfers" is defined as a REQ assertion which coincides with a phase of the P1 signal indicating that valid data is being sent to the initiator.
  - DataOut Phase - Target shall assert P0 before the last 4 REQ edges of the last packet of the stream
- The target may terminate a stream by changing phase or going busfree without having asserted P_CRCA
- Assertion and negation of P_CRCA shall obey the setup and hold time requirements specified in Table 32 of Spi4r0
- The initiator shall use REQ edges to sample the P_CRCA signal.