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REQ/ACK Offsets at Ultra320

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Proposal

- In U320, one clocking signal (REQ or ACK) is a free-running clock. The corresponding signal is used exclusively for flow control - incrementing (REQ) or decrementing (ACK) the current synchronous offset.
- All U320 transfers are information unit transfers and thus are restricted to multiples of two data transfers (32 bits).
- We propose that the handshake signal be modified in U320 such that each edge of the signal requests or acknowledges 32 bits of transfer.

Advantages

- The maximum frequency of the handshake signal would be reduced from 80Mhz to 40Mhz
- The lower frequency reduces ISI and increases the amplitude of isolated pulses. This increases the SNR and decreases the probability of an error.
- Benefits extend to Ultra640 and beyond
- A side benefit is the lower frequency simplifies the reception of this asynchronous signal - you can synchronize at a lower clock frequency

Phase Changes

- The handshake signal can end the transfer in the asserted state. A method for restoring it to the negated state must be provided.
- DataOut Phase:
  - Target changes phase
  - Target waits 2 deskew delays (90ns)
  - Target deasserts REQ
  - Initiator must ignore REQ deassertion after Phase change (NOTE: initiator already must take notice of phase change to stop its free-running clock on ACK)
- DataIn Phase:
  - Target stops free-running clock
  - Target changes phase
  - Initiator negates ACK once phase change detected (within 200ns)
  - Target waits for ACK negation before asserting first REQ of new phase
  - Target must already do this in DataOut where ACK is free-running clock