To: T10 Membership

From: Brian Day, LSI Logic Corporation

Date: 07/07/00

Re: Enhancing performance by reducing training overhead.

It has been shown that in some application environments, the performance impact of additional time during the reestablishment of each I_T nexus can be significant (00-236R0). Although the data was focussed on QAS, the same analysis would apply to the SPI-4 training pattern, currently required to occur on each new I_T nexus. This proposal adds support to allow devices to train less frequently than every physical connection.

PPR Addition

A bit needs to be added to the PPR message to negotiate a Retain Training Information (RTI) bit. An RTI bit of one indicates the vendor-unique training configuration values for each device shall be restored from a previous training sequence prior to the end of selection or reselection.

Description

This additional capability requires no change to the currently proposed SPI-4 training pattern.

An initiator device can establish a retraining condition by initiating a PPR message. This would require targets to always perform training after a PPR message.

A target device is still allowed to initiate a training sequence using the currently defined training protocol by asserting SEL at the reestablishment of the physical connection (regardless of the setting of the RTI bit, the target is still allowed to initiate training as frequently as each connection). The target would still be required to train on the first phase of each direction for that connection.

In the absence of either the PPR message or target assertion of SEL, the training configuration values for each device can be restored prior to the end of the selection/reselection phase. On the completion of any training sequence, the new training values would be used for that connection, and subsequent connections until training is performed again..The starting of the free-running clock would then follow the same requirements as switching between phases later on in a connection.