Proposed Changes for SPI-4 00-246r8

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Associated documents 00-382r0, 00-239r5, 00-320r0 – and after the plenary vote.

Editorial
I really believe the LL (Low Loss) does not work. The NL (Normal Loss) is only a Spec, The I/O cells that I have specified – we are designing and others have designed are actually the Precomp and AAF combined. The higher the speed, the easier it is to have notch or comb filters that are at the operating frequency. The Bloch impedance that Larry Barnes is discovering matches some of the problems I have seen in the field. I believe SPI-5 will require both and some cable and backplane restrictions. Only 30% signals or 70% AC loss in SPI-5 systems will not leave enough amplitude at the receiver for AAF to work. The one major problem left is how to specify timing on a transition that does not reach the zero crossing. No Eye!!! An Example of a SPI-5 problem, the standard Twist and flat cable creates a comb filter the first notch is at 160 MHz, exactly the wrong frequency.

I have left both the normal loss and the no precomp in the proposal, I would like the working group to consider Precomp as specified for the driver with the ability to turn it off and AAF for the receiver. The next working group is October 31, 2000 in Seaside, CA.

The driver/receiver electrical changes proposed for SPI-4

The driver asymmetry equation from the July meeting is wrong. The equations should be Va = (0,9*|Vn|)-23 Minimum and (1,11*|Vn|)+26 Maximum

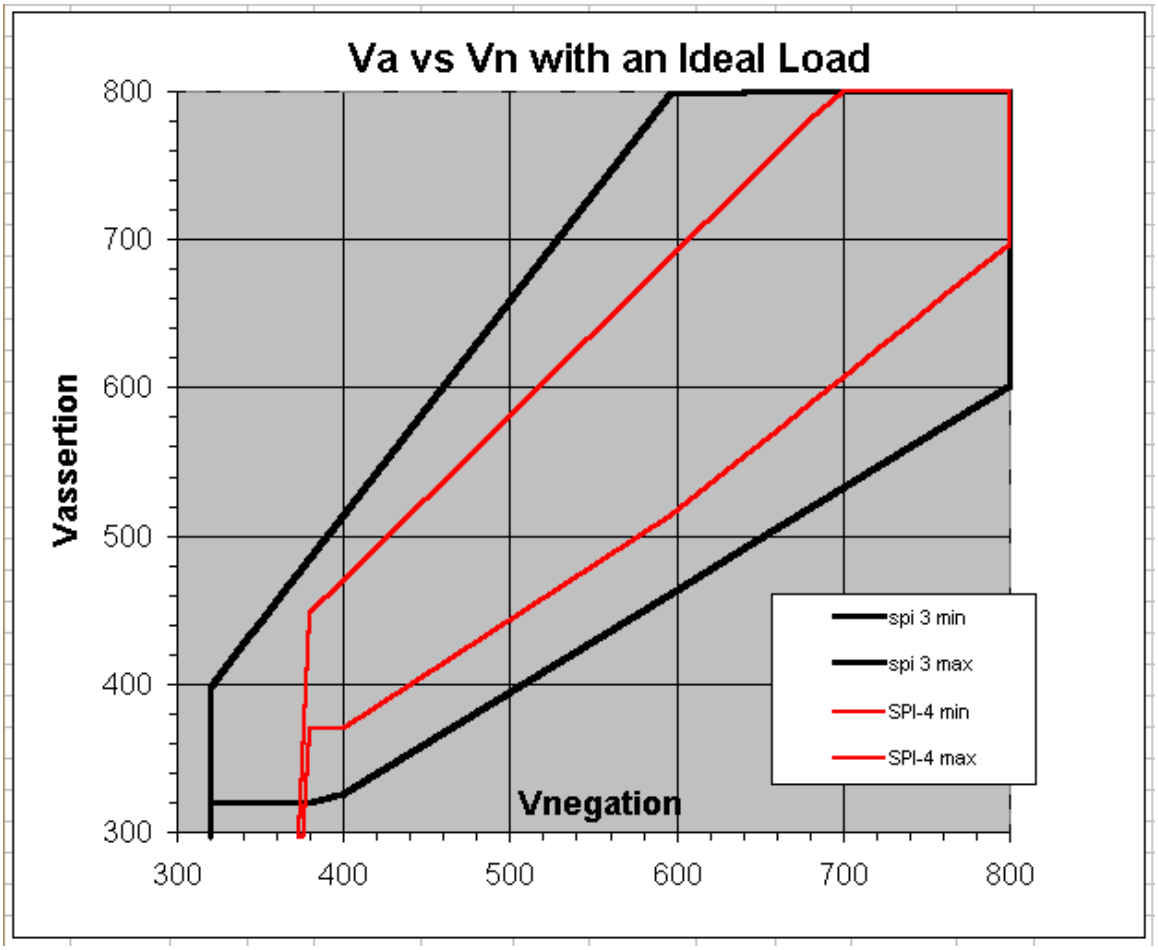
Table A.2 Assertion VA equation for Fast-160 must change to Va = (.9*|Vn|)-23 Minimum and (1.11*|Vn|)+26 Maximum

Change fall back to 50 to 66% from 60 to 78%

A.2.1 Driver requirements overview
The fundamental requirement for an LVD driver is the generation of a first-step differential output voltage magnitude at the driver connections to the balanced media to achieve required minimum differential signals at every receiver connection to the bus. If a P_EN bit of one was received by a SCSI device during the prior PPR negotiation, the weak driver amplitude shall be from a minimum of ~~60~~ 50% to a maximum of ~~78~~ 66% of the strong driver amplitude after the first bit of a series of adjacent ones or adjacent zeros. Other characteristics that affect overall noise margin are the common-mode output voltage, the maximum differential output voltage, the driver output impedance, and the output signal wave shape.

The driver requirements are defined in terms of the voltages and currents depicted in figure 43.

Note: the driver voltage chart must change – New wedge chart.



A.2.2 Differential output voltage, V S

This subclause does not specify requirements for drivers with source impedances less then 1000 Ohms.

To assure sufficient voltage to define a valid logic state at any device connection on a fully loaded LVD bus at least a minimum differential output voltage shall be generated. This value shall be large enough that, after allowance for attenuation (AC and DC), reflections, terminator bias difference, and differential noise coupling, V S is at least +100 mV at the device connector to the LVD SCSI bus. The SCSI device shall also comply with the upper limits for the differential output voltages and to the symmetry of the differential output voltage magnitudes between logic states in order to assure a first-step transition to the opposite logic state. If a PCOMP_EN bit was set to one during the prior PPR negotiation, the signal level at the receiver shall be a minimum of 50 mV Vs on an isolated assertion or negation. Fast-160 without precomp the signal level at the receiver shall be a minimum of –35 mV Vs on an isolated assertion or negation.

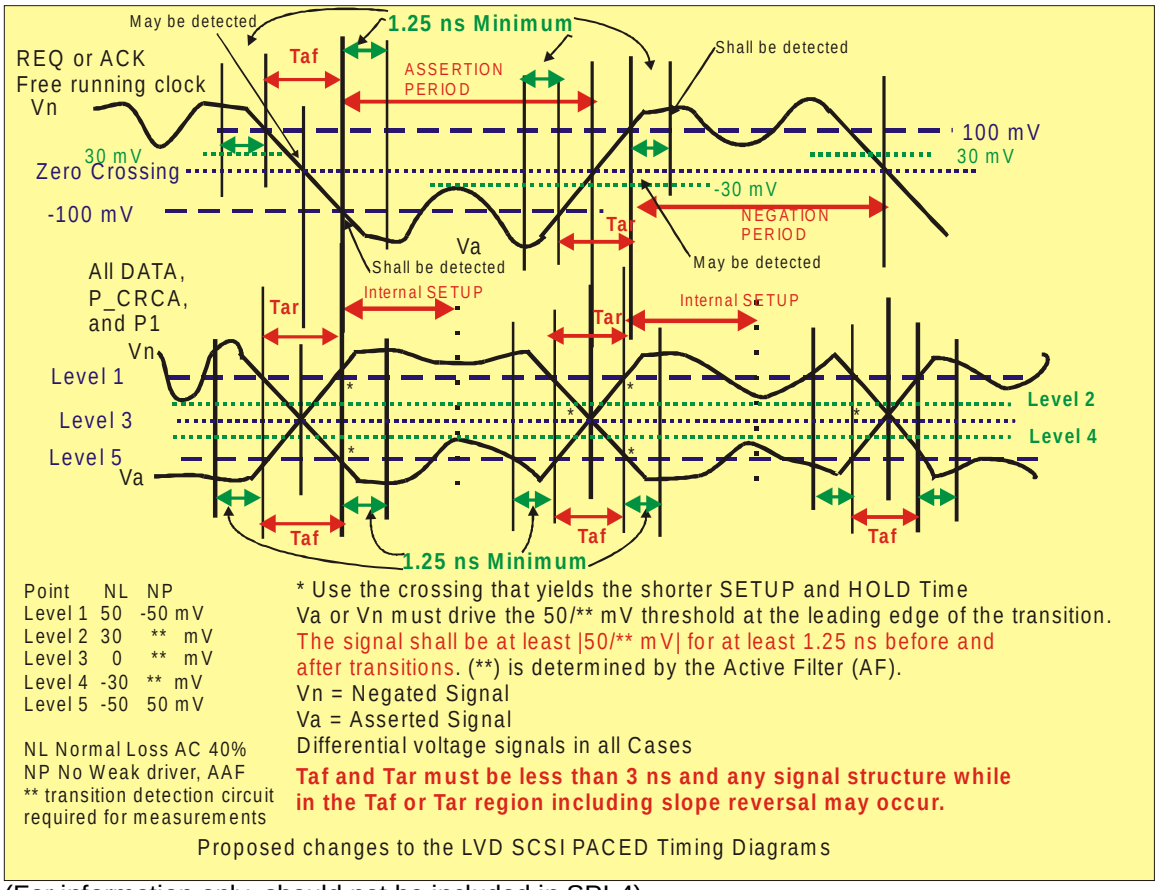
With the test circuit of figure A.1 and the test conditions V1 and V2 in table A.2 applied, the steady-state magnitude of the differential output voltage, V S , for an asserted state (V A), shall be greater than or equal to ~~320~~ 370 mV and less than or equal to 800 mV. For the negated state, the polarity of V S shall be reversed (V N) and the differential voltage magnitude shall be greater than or equal to ~~320~~ 370 mV and less than or equal to 800 mV. The relationship between V A and V N specified in table A.2 for the SPI-2/3 and shown graphically in figure A.2 for the SPI-2/3 shall be maintained. If a P_EN bit was received by a SCSI device during the prior PPR negotiation, the signal level for the strong driver shall be capable of greater than or equal to 500 mV and shall be

less than or equal to 800 mV in the Vn and Va states. The strong driver relationship between V A and V N specified in table A.2 strong driver and shown graphically in figure A.2 for the strong shall be maintained.

The changes are based on the information at the bottom of the first page. 00-382r0, 00-239r5 and SPI-4 R00.

The changes proposed:

Figure 49 Paced Timing diagram and the paragraph under the figure
TBDs replaced a table expect for the free running clock which is 100 mV.



(For information only, should not be included in SPI-4)

Normal Loss (NL) (Proposed –AAF receiver only, this paragraph is for reference only)
The Free running clock shall transition for NL (normal loss systems) from -100 to +100 mV or +100 to -100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. The other signals, the first transition from the multiple bit level shall transition –100 to +50 mV or +100 mV to –50 mV, if there is an immediate transition the +50 mV to –100 mV or –50 mV to +100 mV. The absolute value of the signals shall remain above the 100 mV multiple bits or 50 mV for a single bit level for 1,25 ns at each end of the transition. The absolute value of the signals shall not drop below 30 mV except during the transitions (see 7.3.2).

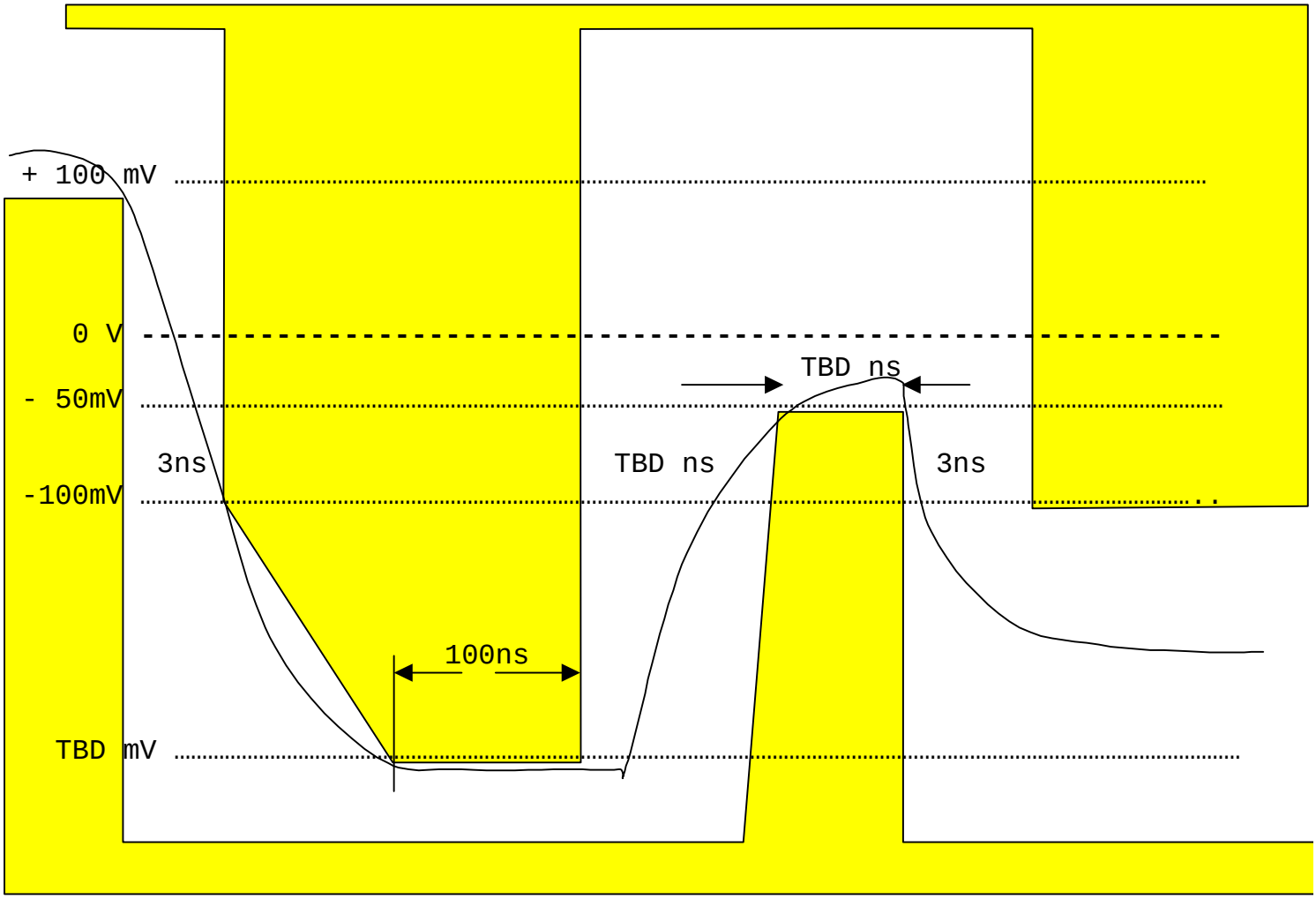
Weak driver off / AAF Adaptive Active Filter (NP)

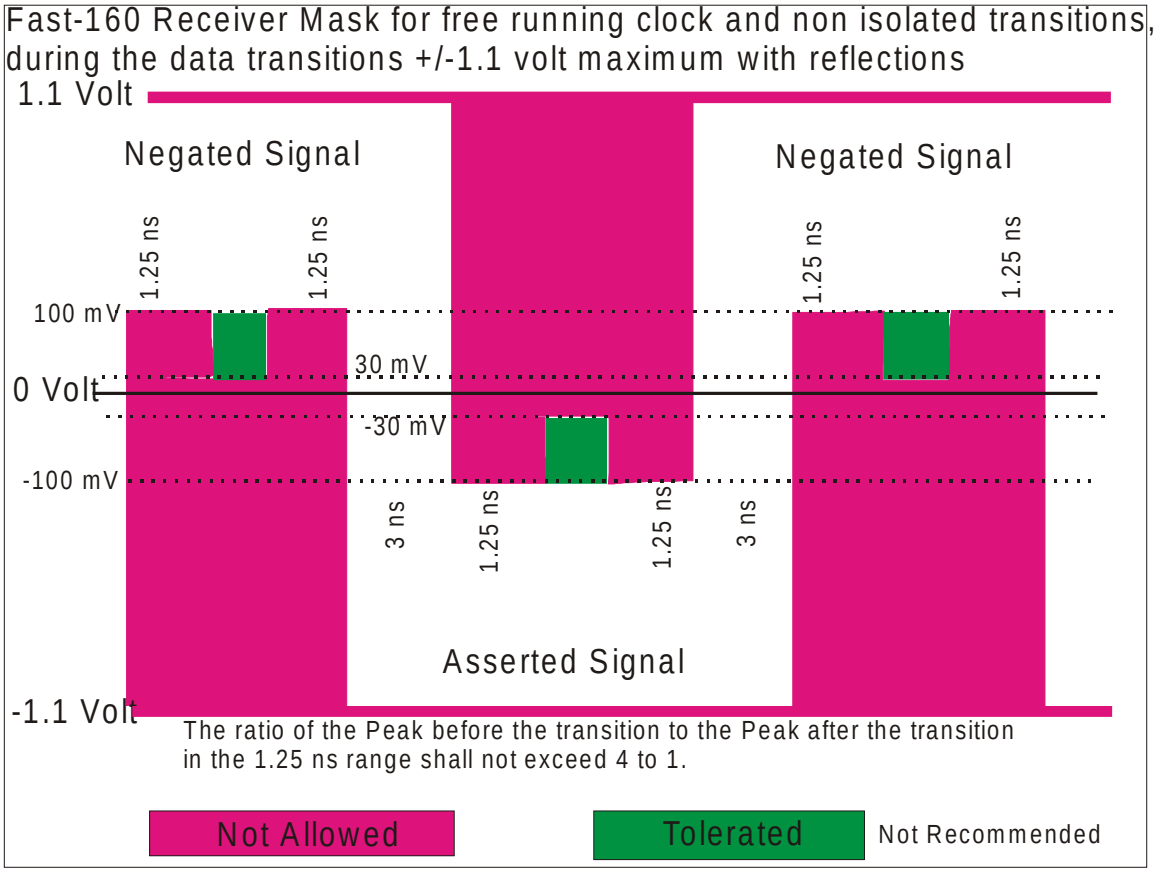
The Free running clock shall transition for NP (no weak driver systems) from -100 to +100 mV or +100 to -100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. The other signals, the first transition from a multiple bit level shall transition at least 200 mV and shall be a minimum 50 mV from the zero crossing, example –300 mV level shall transition to –50 mV for a valid transition.

The absolute value of the multiple bit signals shall remain above the 100 mV for 1,25 ns at each end of the transition. The absolute value of the signals shall not drop below 30 mV except during the transitions (see 7.3.2).

Figure 51 and 52 Receiver Mask paced data transfer

Replaced with Dick Uber's drawing 00-347





Annex A
Table 1
First row maximum -100 mV subsequent bits Fast-160 or all bits Fast-80 or slower
Without precomp enabled maximum 50 mV First bit Fast-160 requires AAF – Note 7

Second row Minimum 100 mV subsequent bits Fast-160 or all bits Fast-80 or slower
Without precomp enabled maximum -50 mV First bit Fast-160 requires AAF – Note 7

Attenuation (%) Fast-160 Maximum 50% Note 5

Note 5 DC Loss 10%, AC loss 40%
Note 6 the free running clock – toggling signal after the first transition must be the 100 mV limits specified by the Fast-80 or slower speeds. These values only apply to isolated transitions.

Note 7 – Weak driver is disabled and AAF (Adaptive Active Filter) receivers used.

Leakage was not consider in V_N (OR-tied signals), leakage can change the bias from the terminators by up to 20 mV

Table A.1 - System level requirements

Parameter	Minimum	Maximum	Cross-reference
V_A (except OR-tied signals) (Except Fast-160 isolated first transition	-1 V	-100 mV	note 1, 6
V_A (except OR-tied signals) (Fast-160 isolated first transition with AAF)	-1 V	50 mV	Note 7
V_N (except OR-tied signals) (Except Fast-160 isolated first transition)	100 mV	1 V	note 1, 6
V_N (except OR-tied signals) (Fast-160 isolated first transition with AAF)	-50 mV	1 V	Note 7
V_A (OR-tied signals)	-3,6 V	-100 mV	note 1
V_N (OR-tied signals)	80 mV	145 mV	note 1, 8
attenuation (%) (fast-40 and fast-80)		15	note 2
attenuation (%) (fast-160)		50	note 5
loaded media impedance (Ohms)	85	135	note 3
unloaded media impedance (Ohms)	110	135	subclause 6.3
terminator bias (mV)	100	125	subclause 7.3.1
terminator impedance (Ohms)	100	110	subclause 7.3.1
device leakage (μA)	-20	20	table 16
number of SCSI devices	2	16	subclause 4.7
ground offset level (mV)	-355	355	note 4

Note:
1 - These are the signal levels at the receiver, the system allows 60 mV crosstalk for calculating the minimum driver level.
2 - Measured from the driver to the farthest receiver.
3 - Caused by the addition of device capacitive load (see table 9 for calculations).
4 - This is the difference in voltage signal commons for SCSI devices on the bus (see figure 3).
5 – Attenuation is the sum of the DC Loss 10% and AC loss 40% at 80 MHz.
6 -The free running clock – toggling signal after the first transition must be the 100 mV limits specified by the Fast-80 or slower speeds. These values only apply to isolated transitions.
7 – Weak driver is disabled and AAF (Adaptive Active Filter) receivers used.
8 - prior versions of the standard did not account for leakage.