

# Proposed Changes for SPI-4

00-246r3

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The driver/receiver electrical changes proposed for SPI-4

The Seagate driver equation from the July meeting is wrong, the tolerance should be 15% without the 57 mV.  $V_a = (V_n \cdot 0.85)$

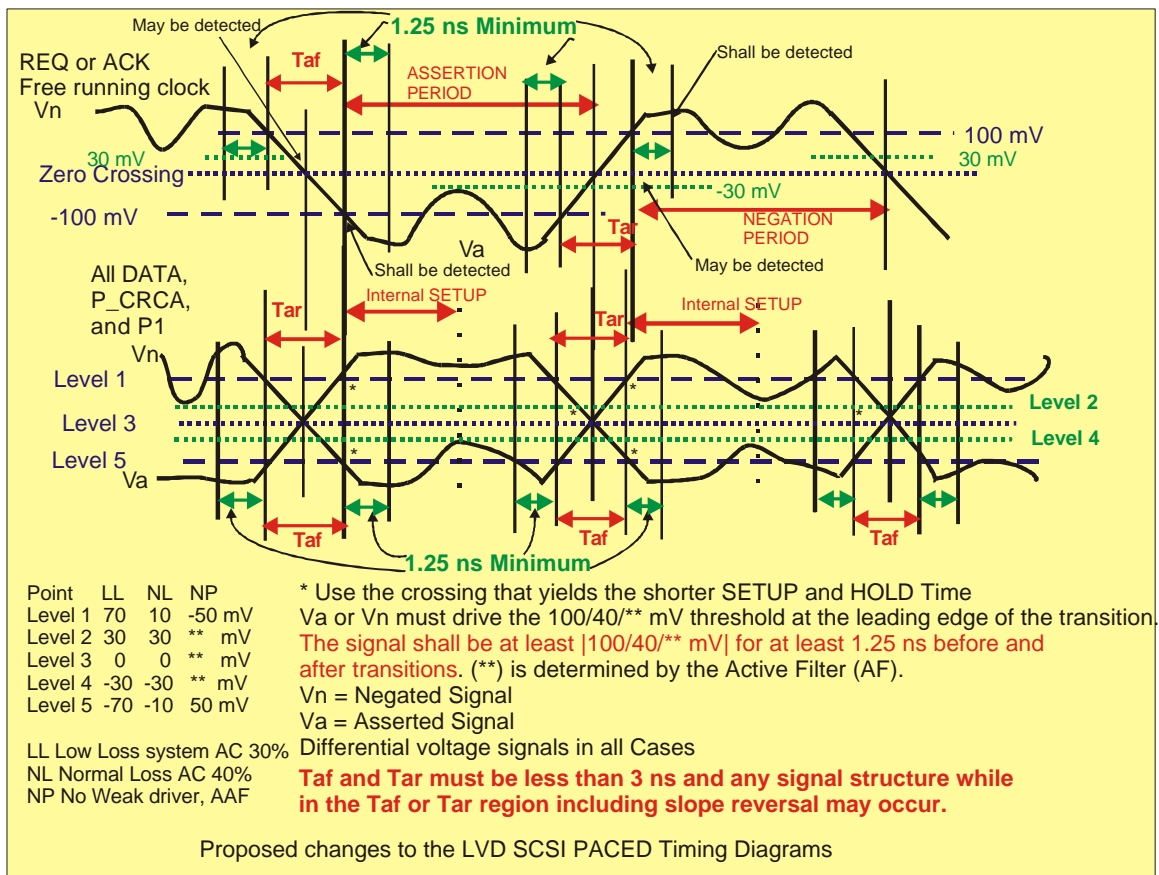
Table A.2 Assertion VA equation for Fast-160 must change to  $V_n \cdot 0.85$  min and  $V_n \cdot 1.15$  Max  
 A.2.2 second paragraph needs an additional clause for Fast-160; If a P\_EN bit was received by a SCSI device during the prior PPR negotiation, the signal level at the receiver may only be 10 mV on an isolated assertion or negation.

The changes are based on the information at the bottom of the first page. 00-227r7, 00-239r3 and SPI-4 R00. Unfortunately there are three camps; Camp 1 - 70 mV receiver requires reducing the cable/system AC loss to 30% with the weak driver, camp 2 - 10 mV receiver AAF recommended the cable/system AC loss 40% (SPI-2/3 losses) with the weak driver and camp 3 - no weak driver and AAF receiver -30mV no zero crossing.

This proposal addresses the three camps.

The changes proposed:

Figure 49 Paced Timing diagram and the paragraph under the figure  
 TBDs replaced a table expect for the free running clock which is 100 mV.



#### Low Loss (LL)

The Free running clock shall transition for LL (low loss systems) from -100 to +100 mV or +100 to -100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. The other signals, the first transition from the multiple bit level shall transition -100 to +70 mV or +100 mV to -70 mV, if there is an immediate transition the +70 mV to -100 mV or -70 mV to +100 mV. The absolute value of the signals shall remain above the 100 mV multiple bits or 70 mV for a single bit level for 1,25 ns at each end of the transition. The absolute value of the signals shall not drop below 30 mV except during the transitions (see 7.3.2).

#### Normal Loss (NL)

The Free running clock shall transition for NL (normal loss systems) from -100 to +100 mV or +100 to -100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. The other signals, the first transition from the multiple bit level shall transition -100 to +10 mV or +100 mV to -10 mV, if there is an immediate transition the +10 mV to -100 mV or -10 mV to +100 mV. The absolute value of the signals shall remain above the 100 mV multiple bits or 10 mV for a single bit level for 1,25 ns at each end of the transition. The absolute value of the signals shall not drop below 30 mV except during the transitions (see 7.3.2).

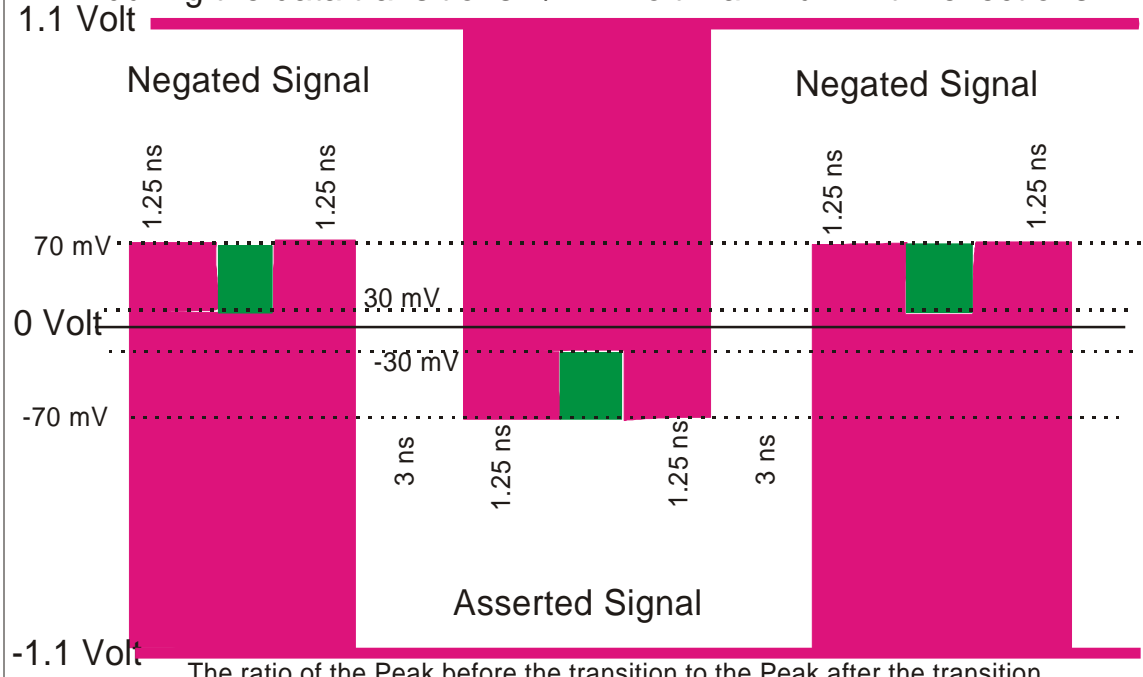
#### Weak driver off / AAF Adaptive Active Filter (NP)

The Free running clock shall transition for NP (no weak driver systems) from -100 to +100 mV or +100 to -100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. The other signals, the first transition from a multiple bit level shall transition at least 150 mV and shall be a minimum 50 mV from the zero crossing, example -200 mV level shall transition to -50 mV for a valid transition.

The absolute value of the multiple bit signals shall remain above the 100 mV for 1,25 ns at each end of the transition. The absolute value of the signals shall not drop below 30 mV except during the transitions (see 7.3.2).

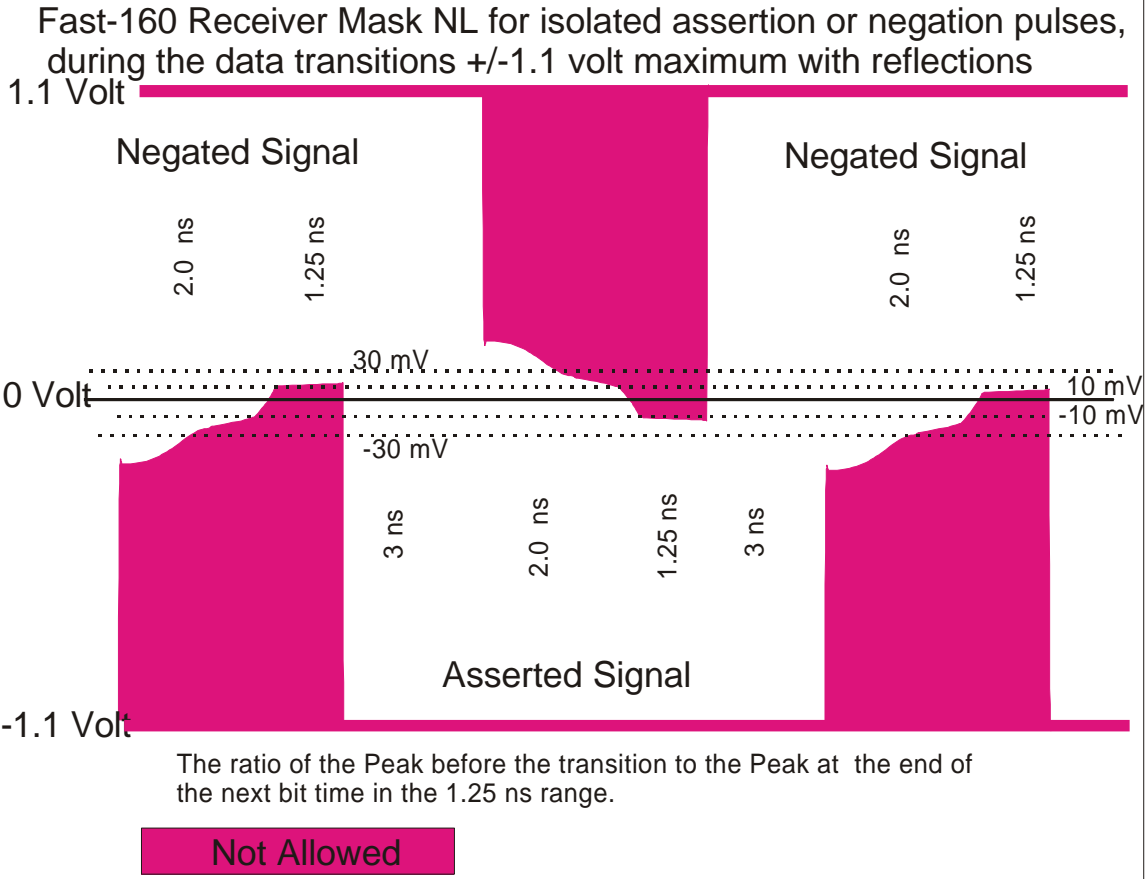
Figure 51 and 52 Receiver Mask paced data transfer needs to be different for the 3 camps, there should be 3 new masks

Fast-160 LL Receiver Mask for isolated assertion or negations, during the data transitions +/-1.1 volt maximum with reflections

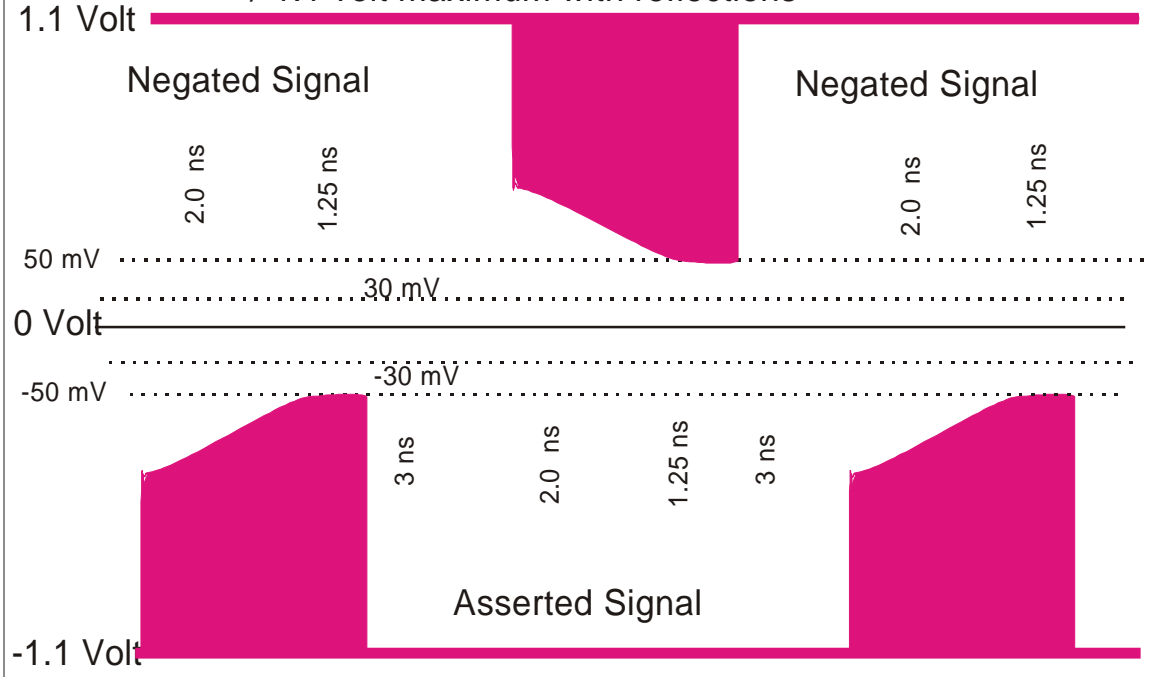


The ratio of the Peak before the transition to the Peak after the transition in the 1.25 ns range shall not exceed 4 to 1.

Not Allowed
Tolerated
Not Recommended



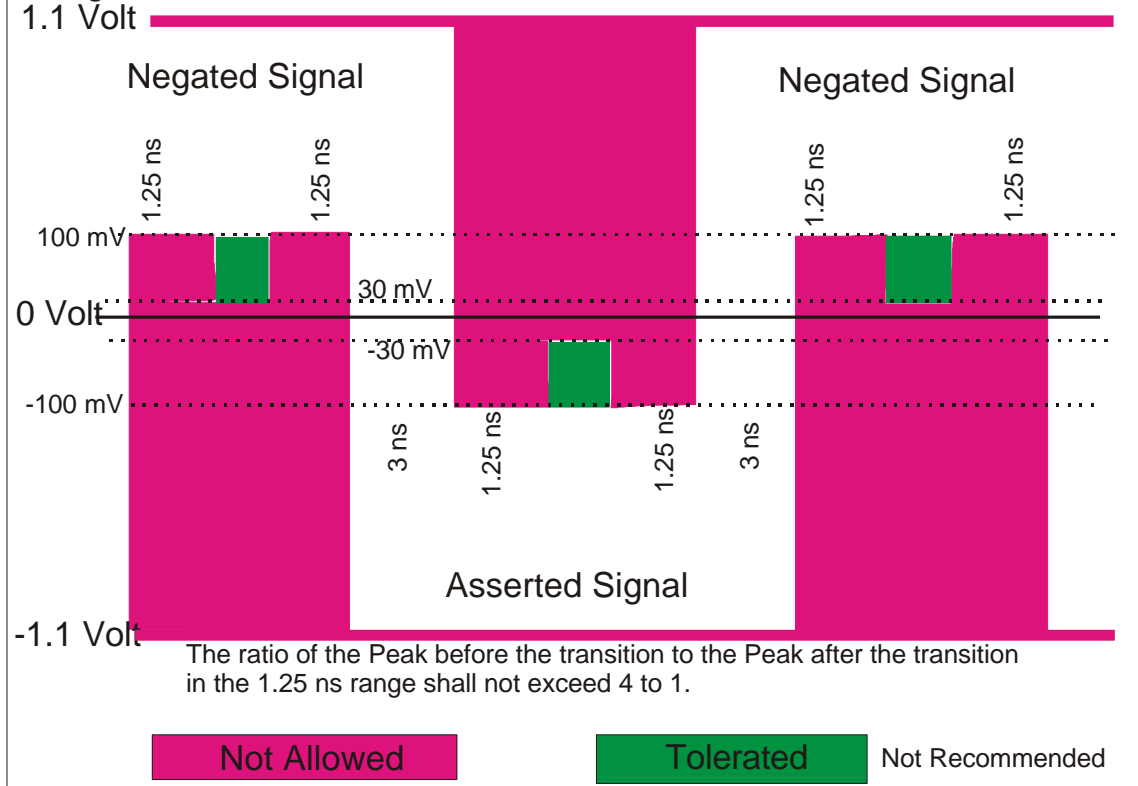
Fast-160 Receiver Mask NP, during the data transitions  
 +/-1.1 volt maximum with reflections



The ratio of the Peak before the transition to the Peak at the end of the next bit time in the 1.25 ns range shall transition 150 mV minimum.

Not Allowed

Fast-160 Receiver Mask for free running clock and non isolated transitions, during the data transitions +/-1.1 volt maximum with reflections



Annex A

Table 1

First row Maximum -10 mV First bit Fast-160 - Note 6

-100 mV subsequent bits Fast-160 or all bits Fast-80 or slower

Without precomp enabled maximum 50 mV First bit Fast-160 requires AAF – Note 7

Second row Minimum 10 mV First Bit Fast-160 – Note 6

100 mV subsequent bits Fast-160 or all bits Fast-80 or slower

Without precomp enabled maximum -50 mV First bit Fast-160 requires AAF – Note 7

Attenuation (%) Fast-160 Maximum 50% Note 5

Note 5 DC Loss 10%, AC loss 40%, if the AC loss is limited to 30% first bit is the same as the subsequent bits.

Note 6 the free running clock – toggling signal after the first transition must be the 100 mV limits specified by the Fast-80 or slower speeds. These values only apply to isolated transitions.

Note 7 – Weak driver is disabled and AAF (Adaptive Active Filter) receivers used.

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Leakage was not consider in V<sub>N</sub> (OR-tied signals), leakage can change the bias from the terminators by up to 20 mV

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**Table A.1 - System level requirements**

Parameter	Minimum	Maximum	Cross-reference
V <sub>A</sub> (except OR-tied signals) (Except Fast-160 isolated first transition)	-1 V	-100 mV	note 1
V <sub>A</sub> (except OR-tied signals) (Fast-160 isolated first transition with precomp)	-1 V	-10 mV	note 5
V <sub>A</sub> (except OR-tied signals) (Fast-160 isolated first transition with AAF)	-1 V	50 mV	Note 7
V <sub>N</sub> (except OR-tied signals) (Except Fast-160 isolated first transition)	100 mV	1 V	note 1
V <sub>N</sub> (except OR-tied signals) (Fast-160 isolated first transition with precomp)	10 mV	1 V	note 5
V <sub>N</sub> (except OR-tied signals) (Fast-160 isolated first transition with AAF)	-50 mV	1 V	Note 7
V <sub>A</sub> (OR-tied signals)	-3,6 V	-100 mV	note 1
V <sub>N</sub> (OR-tied signals)	80 mV	145 mV	note 1
attenuation (%) (fast-40 and fast-80)		15	note 2
attenuation (%) (fast-160)		50	note 6
loaded media impedance (Ohms)	85	135	note 3
unloaded media impedance (Ohms)	110	135	subclause 6.3
terminator bias (mV)	100	125	subclause 7.3.1
terminator impedance (Ohms)	100	110	subclause 7.3.1
device leakage (μA)	-20	20	table 16
number of SCSI devices	2	16	subclause 4.7
ground offset level (mV)	-355	355	note 4

Note:

- 1 -These are the signal levels at the receiver, the system allows 60 mV crosstalk for calculating the minimum driver level.
- 2 -Measured from the driver to the farthest receiver.
- 3 -Caused by the addition of device capacitive load (see table 9 for calculations).
- 4 -This is the difference in voltage signal commons for SCSI devices on the bus (see figure 3).
- 5 -DC Loss 10%, AC loss 40%, if the AC loss is limited to 30% first bit is the same as the subsequent bits.
- 6 -The free running clock – toggling signal after the first transition must be the 100 mV limits specified by the Fast-80 or slower speeds. These values only apply to isolated transitions.
- 7 – Weak driver is disabled and AAF (Adaptive Active Filter) receivers used.

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Below accepted in the July 2000 meeting

3<sup>rd</sup> row Maximum –100 mV

(This is wrong and needs to be changed to 0,85 x V<sub>n</sub> min and 1,15 x V<sub>n</sub> max)

Table A.2 last line remove TBD and use the old values with a Note for Fast-80DT and slower  
Add a new line for Fast-160 Min 0,85 x |V<sub>n</sub>|+50 Max 1,15 x |V<sub>n</sub>| -57