Proposed Changes for SPI-4

00-246r1

Paul Aloisi TI

The communications to date shows that it is possible to tighten up the driver specification which will leave an eye for the receiver. I have not worked out the details for the receiver mask, but it has to be different than it is draw now.

The changes are based on the information at the bottom of the first page. 00-227r4 and SPI-4 R00.

The changes proposed:

Figure 49 Paced Timing diagram and the paragraph under the figure
TBDs replaced with –40 and +40 mV

Figure 51 and 52 Receiver Mask paced data transfer
needs work, it needs to be show for the first transition and subsequent transitions.

Annex A
Table 1
First row Maximum -40 mV First bit Fast-160
-100 mV subsequent bits Fast-160 or all bits Fast-80 or slower

Second row Minimum 40 mV First Bit Fast-160
100 mV subsequent bits Fast-160 or all bits Fast-80 or slower

3 rd row Maximum –100 mV

Table A.2 last line remove TBD and use the old values with a Note for Fast-80DT and slower
Add a new line for Fast-160 Min 0,85 x |Vn|+50 Max 1,15 x |Vn| -57