

SPI-4 Assumptions for the Receiver and Driver levels

00-239r6

Paul Aloisi

October 2000

These are the assumptions that the receiver timing diagrams and driver levels are based on for SPI-4. These were all discussed in 00-227 at the August 2000 meetings which generated the new version of the timing diagrams, receiver requirements and drive levels. 00-382r0 shows the new levels.

1. All measurements are at the device connector.
2. Receivers have a +/-30 mV DC offset.
3. 10% DC loss from terminator tolerance, DC loss and connectors
4. 40% AC loss at 80 MHz over the DC signal level
5. Drivers for first transition drives strong, after the first bit the drive level drops to the weak driver 50 to 66% of the strong driver. The strong driver must be greater than or equal to 500 mV less than or equal to 800 mV. Drivers must meet the asymmetry balance $(0.9 * V) - 23$ or $(1.11 * V) + 26$.
6. System noise and crosstalk is 60 mV
7. The signal left for the receiver meeting all the requirements above and the same cable-backplane plant in SPI-3 levels. The first pulse or transition will only reach 50 mV at the receiving device connector with Precomp. Receivers should work with signals that just reach the zero crossing to provide some margin. If precomp is disabled and AAF (Adaptive Active Filter) receivers are used, the receivers must work with signals that do not reach zero crossing. Receivers should work with a transition of at least 150 mV, that come within 50 mV of zero crossing. Note; this works over a much greater loss than the other systems.
8. Receivers shall reject high frequency noise.
9. Training pattern required for adaptive active filter calibration and skew compensation.