SPI-4 Assumptions for the Receiver and Driver levels

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These are the assumptions that the receiver timing diagrams and driver levels are based on for SPI-4. These were all discussed in 00-227 at the July 2000 meetings which generated the new version of the timing diagrams, receiver requirements and drive levels.

1. All measurements are at the device connector.

2. Receivers have a +/-30 mV DC offset.

3. 10% DC loss from terminator tolerance, DC loss and connectors

4. 40% AC loss at 80 MHz over the DC signal level.

5. Drivers for first transition drives strong, after the first bit the drive level drops to the weak driver 60 to 78% of the strong driver. The weak driver must be greater or equal to 320 mV, the strong driver must be less than or equal to 800 mV. Drivers must meet the asymmetry balance ((0.85 * V)+50).

6. System noise and crosstalk is 60 mV

7. The signal left for the receiver meeting all the requirements above and the same cable-backplane plant in SPI-3 levels. The first pulse or transition will only reach 40 mV at the receiving device connector with Precomp. Receivers should work with signals that just reach the zero crossing to provide some margin.

8. If precomp is disabled and AAF (Adaptive Active Filter) receivers are used, the receivers must work with signals that do not reach zero crossing. Receivers should work with a transition of at least 150 mV, that come within 100 mV of zero crossing.

9. Receivers must have an active filter that will allow 80 MHz signals that only reach zero crossing when system noise and crosstalk is considered, to be a valid signal. This requires an active filter that will boost the high frequency (80 MHz) signals up to 2X the DC level.

10. Receivers must reject high frequency noise, 3 times the fundamental (Fast-160 – 80MHz, 240 MHz must be rejected).

11. Training pattern required for adaptive active filter calibration and skew compensation.