

SCSI signal modeling study group (SSM)  
June 13, 2000  
Lisle, IL

00-218r1

Subject: Approved minutes for the SSM working group on April 12, 2000 in Milpitas, CA

This was the next meeting to address the general subject of modeling for parallel SCSI. Dean Wallace of Q Logic led the meeting. Bill Ham of Compaq took these minutes. There was a good attendance from a broad spectrum of the industry. Adaptec (Tariq Abou-Jeyab) hosted the meeting.

Last approved minutes: 00-164r1.

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## 2. Introductions

Dean Wallace opened the meeting and conducted the introductions and reviewed the meeting purpose. He thanked Tariq Abou-Jeyab of Adaptec for hosting the meeting.

## 3. Attendance

The following folks were present:

## 4. Attendance

The following folks were present:

Name	Company	E-Mail
Tariq Abou-Jeyab	Adaptec	tajeyab@corp.adaptec.com
Paul Aloisi	TI	Paul_Aloisi@ti.com
Larry Barnes	LSI	larry.barnes@lsil.com
Umesh Chandra	Seagate	Umesh_chandra@notes.seagate.com
Dave Chapman	Amphenol	dave.chapman@aipc.fabrik.com
Jason Chou	Foxconn	jasonc@foxconn.com
Jie Fan	Madison Cable	jfan@madisoncable.com
Bob Gannon	JPM	rgannon@jpmco.com
Bill Gintz	Zeus	wegintz@ix.netcom.com
Bill Ham	Compaq	bill_ham@ix.netcom.com
Lee Hearn	Adaptec	lee_hearn@corp.adaptec.com
Thom Kreusel	HP	thom_kreusel@hp.com
Larry Lamers	Adaptec	ljlammers@corp.adaptec.com
David MacQuown	Adaptec	david_macquown@corp.adaptec.com
Bruce Manildi	Seagate	bruce_manildi@notes.seagate.com
Martin Ogbuokiri	Molex	mogbuokiri@molex.com
Mario Sahaguna	JPM	msahagun@jpmpantera.com
Matt Schumacher	Compaq	matt.schumacher@compaq.com
Dan Smith	Seagate	daniel_f_smith@notes.seagate.com
Greg Vaupotic	Amphenol	greg.vaupotic@snet.net
Dean Wallace	Qlogic	d_wallace@qlc.com

#### 5. Agenda development

The agenda shown was that used.

#### 6. Approval of previous minutes

The minutes of the last meeting were reviewed and minor changes were made. Bill Ham moved and Dan Smith seconded that these revised minutes be approved. Motion passed unanimously. This document will be posted as document 00-164r1.

#### 7. Action item review

The action items were reviewed with the status indicated in the action item section of the minutes.

#### 8. Presentation Policy

This item is included for easy reference and will be retained in future minutes.

It is the policy of the SSM working group that all material presented at the SSM working group shall be made available electronically and posted on the T10 web site.

Material presented at the meeting should be uploaded to the T10 web site two weeks prior to the meeting. Alternatively the material may be electronically supplied to the chair or secretary at the meeting where the material is presented at the discretion of the chair.

Material should be free from any statement of confidentiality or restriction of use and should not contain any pricing or product scheduling information.

#### 9. Document review - Barnes

No specific output since last meeting. Larry has now acquired his very own notebook computer which will be available in future meetings for real time editing.

Some framework editing will be done in the later agenda item relating to the framework for the document.

It was suggested that the June meeting be used mainly for editing the document (assuming that significant new input is received by Larry).

## 10. Presentations

### 10.1 SPIP status - Dave Chapman / Ham

Bill Ham reviewed the work done in the SPIP group on Tuesday. See the minutes for the SPIP meeting for the details. There is very significant interaction needed between the SPIP and SSM groups especially in the areas of resonance and interoperability points.

### 10.2 Industry overview - Ham

See 00-178r0 for the details.

### 10.3 Multidrop cable assemblies - group

Deferred to the June meeting.

### 10.4 Transition region model plan - Gannon

Bob presented a live demonstration (running on his notebook computer) of the Maxwell Q3D extractor for an IDC flat ribbon cable type of construction. There was a discussion of the peculiarities of the Ansoft package with respect to the terms "source" and "sink". It requires special skills to describe the setup for the model.

There are many subtleties in using this kind of tool which clearly illustrate the critical importance of verification.

A discussion of whether there should be a defined owner for the complete cable assembly produced the agreement that the focus should be on the connector, transition region, and cable media for now and that the integration of these into a complete cable assembly model will be done later (if at all).

Greg Vaupotic and Bob Gannon will get together off line and come up with a joint proposal for the twist and flat transition region modeling approach with results.

Larry Barnes recommended that the Q3D Ansoft tool is probably the best tool for most applications presently facing the SSM group.

Other specific suggestions from the last meeting are retained in the minutes until placed in the document. See following:

Thoughts on transition region variables: How do we define the transition region and what are the parameters that define the transition region? The region runs from the point of cutting the bulk cable to the point of being loaded on the connector. The shielding is different in transition region than on cable. What is fanout extent?

SCSI Cables- Internal and External, round shielded, round unshielded, flat cable, twist and flat are all different.

Connectors- 25 position std SCSI, 34 position std SCSI, 25 & 34 position .8 mm, Internal IDC, Straddlemount, 0.8 mm, Offset 0.8mm each have different physical parameters

IDC- Insulation pierce, deformation of plastic, stress on contacts, flaking of tin, change in conductivity may affect the performance

Paddlecard attach- Reflow of solder, wire to solder pad attach, different solder characteristics

Crimp and poke- Crimp tools/applicators, plating thickness of contacts, applicator geometry, points of contact to wire, pull force versus resistivity

Model Options:

Ansoft Maxwell 2D and 3D Modeler

Pacific Numerix/Ansoft

HP ADS

IFS Connect/Interaction Products

Cascaded Models

Concerns- Frequency characteristics of dielectrics, accuracy of lumped parameter models, Changes in lumped parameters with respect to frequency. This has to be a distributed model for all cases except possibly IDC to flat.

Other Resources- Outside consultants, Pre-existing work

Action Items- Produce matrix of transition regions and issues with each.

Moving Forward- What should be timetable, Action items for next meeting

## 11. Matrix development for SSM

The following summarizes the present position for the SSM matrix. This matrix is a concise description of the methodology to be used for the respective areas of the point to point SCSI bus segment. Several of the

areas were significantly modified at this meeting. Note that the multidrop areas have not yet been identified.

This section contains some repeated information from the last minutes as it continues to be relevant and current.

#### 11.1 Transceiver chips: owner, Dean Wallace

No new content info this meeting.

Interface is at packaging pins

Model types: Spice, IBIS, HDL, table spice - details TBD

Data patterns: TBD

ISI compensation: required but not presently believed compatible with IBIS capability - this means that IBIS will have to be enhanced and that only SPICE models will be effective until the new IBIS techniques are available.

Single line required - cross talk from non SCSI sources not considered in the model, SCSI line cross talk is not significant within the transceiver. Therefore multilane models are not required for transceivers.

Action Item: Dean to email folks who have open action items relating to transceivers.

#### 11.2 Bus segment termination: owner, Paul Aloisi / Don Getty

No new content information.

Interface is at package pins

Model types: Spice, IBIS details TBD

Terminator type: multimode

Single line only

#### 11.3 Transceiver board: owners, Tariq Abou-Jeyab and Matt Schumacher

No new content information.

Interface is at transceiver board connectors, transceiver chip pins, terminator chip pins

Model types: Spice

PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities

Single line, multilane

The present paradigm for this component follows:

Listed are some key datapoints to consider for HSPICE simulation of a simple LVD SCSI PCB. Initial simulations will be used to optimize PCB routing topologies. Simulating worst case scenarios will be discussed in a later document, as it will require SPICE model correlation, process corners, multiline SPICE models for cross talk etc.

**Request SPICE models:**

check for a driver and a receiver model  
Ask for single line models and multiline models of connectors. Multiline models may take much longer to arrive if you can get them at all. If single line models are used, signal integrity investigation will not include crosstalk.  
Are models for unmated connectors necessary?  
Required models must work for various edge rates (slow, typ, fast)  
Keep the models in a centralized/secure location. Vendors usually distribute them under NDA.  
Some correlation of the models is recommended (compare simulation and lab data)  
Request models well in advance of need

**Obtain transmission line geometries from PCB data / design requirements**

These parameters are required: trace width, copper weight of trace and planes, dielectric constants, dielectric spacing within the differential pair, dielectric spacing to the planes and trace lengths of the nets to be simulated.

**Generate RLGC matrices for transmission line segments(cline):**

Using a field solver, obtain the RLGC matrices for the transmission line geometries.  
Compare the field solver impedance with the TDR measurement of the coupon.  
Note: the coupon will provide a controlled environment with minimal discontinuities for accurate trace characterization.

**Draft a trace topology from the known trace segments and components:**

Draft the transmission line topology  
the drawing below is an example of a simple transceiver board in host bus adapter

**Build a spice netlist for the trace topology:**

Do not forget the process variations.

**Simulate and review data:**

Time domain simulation is sufficient for optimizing topologies.  
W's are SPICE element numbers. All other numbers are node locations.

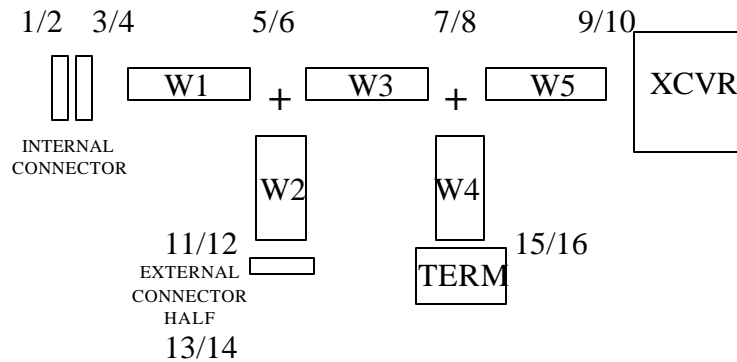


Figure 1 - Architecture of a transceiver board model (no unused connectors)

#### 11.4 Mated connectors: owner, Martin Ogbuokiri

No new content information.

Interface is at transceiver board and the cable assembly transition region

Model types: Spice

Connector types: VHDCI, SCA-2, HD68

Mounting style: thru hole, SMT, single line, multilayer

Connector models are in place at the Molex web site and pointers are now in place on the T10 site.

#### 11.5 Cable assembly transition region: owners, Bob Gannon, Greg Vaupotic

Interfaces are at the connector termination and the uniform media

Model types: Spice same as connector

Construction types: twisted flat, round fanout, laminated round, IDC flat?

Single line multi-line

A start was made in this area - see Bob Gannon presentation above.

#### 11.6 Uniform cable media: owner, Jie Fan

Interfaces are at the beginning of the cable assembly transition region on either end.



Model types: Spice

Cable types: flat, round shielded, round unshielded twisted flat?

Single line, multiline

Hitachi agreed to become a co-owner of this matrix element.

Action item: Jie to provide a cable media model to the web site.

#### 11.7 Backplane: owner, Larry Barnes

Interfaces: connectors mounted on the backplane, directly mounted components,

Model types: SPICE

PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities

Single line, multiline

Issue: how to handle the unmated connectors on the backplane. Two sub issues: (1)lack of existence of unmated connector models and (2) convergence of the simulation with dangling open circuits. The latter can be handled by adding a high value resistance to the open circuit to "fool" the simulator.

Action item: Larry Barnes to supply component definition and a graphical representation for the backplane (should not contradict the transceiver board if possible)

#### 12. Simulation integration strategy

Further discussion pending progress on the component level simulation work. This will be addressed at the next meeting.

#### 13. System configurations

Not discussed but reaffirmed as needed for the document

#### 14. Data patterns

A preliminary discussion of the issues involving data patterns was held. The following resulted:

Data patterns need to consider the following properties:

- Intersymbol interference effects on single lines

- Cross talk from other SCSI lines
- driver release effects (driven to hi Z)
- Residual jitter (clock like patterns)
- Word patterns as well as individual patterns
- SSO
- Worst case digital patterns
- Sinusoidal patterns
- Resonance sensitivity

A spirited discussion concerning how to deal with receivers that modify the input signal (either adaptively or not) was held. Is this part of the signal path or not?

A more general concept of data pattern is possible with simulation because the inputs can be selected in the model. For example, skew from line to line and skew within the same line can be introduced. This latter was not considered in any detail but promises to be a significant benefit of modeling.

#### 15. Data rate

Data transfer rates in SCSI are determined by more than the highest frequency content of the signals. Specifically, single transition, double transition, width, specific protocol variant and adaptive filtering affect the data rate. Therefore one must be careful in simulation to ensure that the relationship between the analog signals and the application is understood.

The following table will be added to the document that shows some of the relationships:

SCSI variant	REQ/ACK maximum frequency (MHz)	Data line maximum frequency (MHz)	Minimum rise / fall time (ns) (20-80%)	Maximum launch amplitude
SCSI-1 SE	async - NA	NA	NA	5.25V
SCSI-2 SE	5 MHz	2.5 MHz	NA	5.25V
SPI-1 SE	10 MHz	5 MHz	5 ns	5.25v
Ultra SE	20 MHz	10 MHz	5 ns	3.7v
Ultra2 LVD	40 MHz	20 MHz	1 ns	2.2 V DFpp
Ultra 160 LVD	40 MHz	40 MHz	1 ns	2.2 V DFpp
Ultra 320 LVD	80 MHz	80 MHz	1 ns	2.2 V DFpp
Ultra 640 LVD	160 MHz	160 MHz	???	???

## 16. Definitions:

A comprehensive set of definitions has been created in the draft document. Definitions from IEEE standard dictionary are used if available.

## 17. Model database strategy (Wallace)

The revised proposed a specific summary of the present plans for the web based database:

- List of companies with existing models.
- What type of models are they. Connector media, transceiver etc.
- Description / intended use
- Path to the model, is an nda required for the model
- Contact info for model support
- What type of model, SPICE, IBIS, HDL.
- Revision history on site.

Martin noted that he intends to use a no fee license rather than an NDA for access to Molex models identified by the T10 web site.

Larry called for drafting a generic no fee license for all suppliers of models. Martin agreed that the SSM group may use their no fee license as a starting point.

## 18. Tools:

This item refers to software tools that may be useful for SSM.

Note that IBIS is not a tool but rather is a behavioral specification for I/O buffers and other stuff such as terminators and connectors. IBIS is described separately.

Following is a list of the major tools and the basic relationship between them:

Simulation tools:

- SPICE-like
  - HSPICE
  - Berkeley SPICE
  - Contec SPICE
  - PSPICE

- Behavioral
  - HDL

VHDL  
Verilog  
Hyperlynx  
Viewlogic XTK

High frequency structural simulator  
Ansoft  
HP-ADS (advanced design simulator)

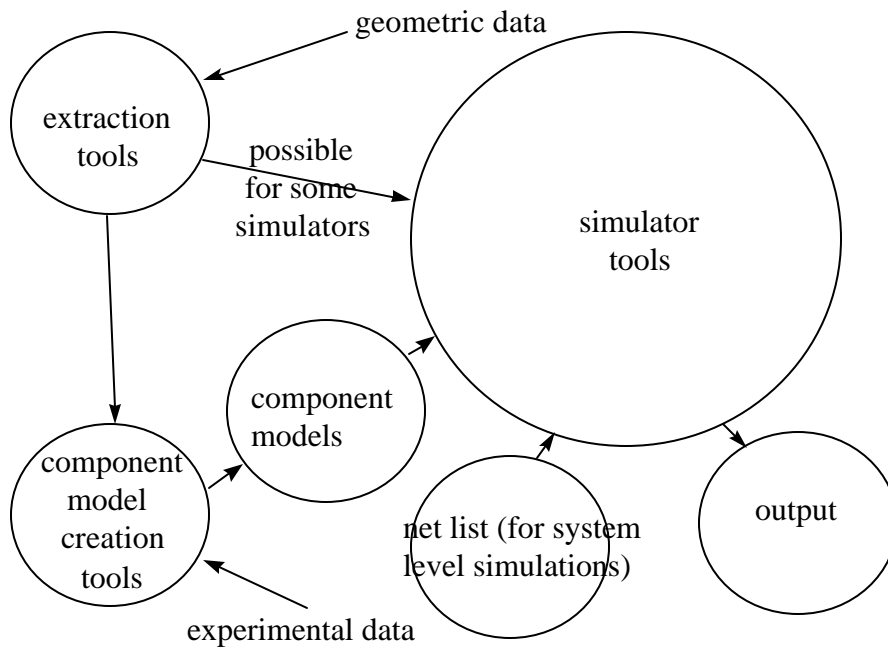
Extraction tools

Maxwell  
Maxwell-2D  
Maxwell-3D  
Pacific Numerix

Model creation tools

Mentor Graphics  
Cadence  
HP suite

The following figure shows the relationship between the different tool classes:



## 19. Document framework (Barnes)

Larry Barnes, editor of the SSM document presently posted as 99-204r0, reviewed the present state and organization of the document. Following is the result of this discussion cast in the form of a table of contents with owners assigned. The numbering may not be accurate in the list below. Note the addition of Dima to the cable assemblies section.

Section owners are to create basic material and submit to Larry Barnes before the next meeting.

1. SCOPE ((Larry Barnes - 100%)
2. REFERENCES
  - 2.1 Approved references
    - 2.1.1 References under development
3. Resources
  - 3.2.1 Publications (Jonathan Fasig - 100%)
- 3.3 Tools (group - 80%)
4. DEFINITIONS, ACRONYMS, SYMBOLS, KEYWORDS, AND CONVENTIONS (group)
  - 4.1 Definitions (20%)
  - 4.2 Acronyms (80%)
  - 4.3 Symbols and Abbreviations (100%)
  - 4.4 Keywords (100%)
  - 4.5 Conventions (100%)
  - 4.6
- 5.0 General / Overview (Bill Ham - 50%)
6. Methodology
7. MODELS
  - 7.1 General recommendations (Larry Barnes - 10%)
    - 7.1.1 Supporting documentation
    - 7.1.2 Behavioral models
    - 7.1.3 Circuit Models
  - 7.2 Cables
    - 7.2.1 Cable media (bulk cable) (Jie Fan / Zane Daggett - 10%)
    - 7.2.2 Transition region (Bob Gannon, Greg Vaupotic - 10%)
  - 7.3 Connectors (Martin O. - 5%)
    - 7.3.1 Cable connectors
    - 7.3.2 Non-cable connectors
      - 7.3.2.1 RLC transmission line matrix
  - 7.4 Printed circuit boards (Matt S., Tariq A. - 30%)
    - 7.4.1 Traces
      - 7.4.1.1 Microstrip
      - 7.4.1.2 Stripline
      - 7.4.1.3 Broad coupled stripline
      - 7.4.1.4 Offset broad coupled stripline
    - 7.4.2 Discontinuities
      - 7.4.2.1 Vias
      - 7.4.2.2 Pads
  - 7.5 Devices
    - 7.5.1 Terminators (Paul Aloisi / Don Getty - ?)
    - 7.5.2 Transceivers (Dean Wallace - 5%)
    - 7.5.3 Packages (Larry Barnes - 5%)
8. STANDARD MODEL CONSTRUCTIONS

- 8.1 Host bus adapter / target board (Tariq / Matt S. - 70%)
- 8.2 Point to point cable assemblies (Dima Smolyansky - 40%)
- 8.3 Multidrop cable assemblies (TBD)
- 8.4 Backplane (Larry Barnes - 10%)
- 8.5 System model (group - 2%)
- 9. VALIDATION PROCEDURES
  - 9. Physical measurement points (Greg Vaupotic)
    - 9.1 Access to measurement points (Larry Barnes / Martin O.)
    - 9.2. device connector
      - 8.2.2 chip to board interface
      - 9.2.3 terminator connector
    - 9.3 Instrumentation input models (Jason Chou - 5%)
      - 9.3.1 scope probe models
      - 9.3.2 network analyzer models
      - 9.3.3 test port cables
      - 9.3.4 instrument transfer function
    - 9.4 Use of frequency / time domain for validating elements of component models (
    - 9.5 Distributed vs lumped resonance issues
    - 9.6 Behavioral
    - 9.7 Circuit
  - 10. SIMULATION INTEGRATION STRATEGY (Dean Wallace)
    - 10.1 System configurations
    - 10.2 Data patterns
    - 10.3 Data rates

## 20. New business

No new business was conducted.

## 21. Next meetings

Scheduled meetings:

June 13-14, 2000 1:30PM to 5PM 6/13 9AM to 5:00PM 6/14, Lisle, IL  
(Molex)

Requested meetings:

August 15-16, 2000 1:30PM to 5 PM 8/15 9AM to 5PM 8/16, Colorado Spgs  
(LSI logic)

October 12-13, 2000 1:30PM to 5PM 10/12 9AM to 12:00PM 10/13, Santa  
Cruz, CA (Seagate)

## 22. Action Items:

## 22.1 Action items from previous meetings

Status as of the April 12, 2000 meeting is shown.

Larry Barnes to propose a multilevel output capability for IBIS to allow for ISI compensation.

Status: done for multilevel in IBIS 3.2

Larry Barnes will hatch a BIRD at IBIS to incorporate ISI compensation as defined by SPI-4 when SPI-4 stabilizes.

Status: transformed from old action item - on hold pending SPI-4 resolution

Action item: Dan Smith to provide access information for the Seagate transceiver models to the web site.

Status: IBIS models are intended to be made available but there is concern about the accuracy of the model in its present state - see Larry Barnes action item below -- carried over

Larry Lamers to provide access information for the Adaptec transceiver models to the web site.

Status: IBIS models now exist but there is reluctance within Adaptec to release the models to the T10 web site because of concern about the IP contained in the model, Adaptec intends to provide appropriate models after due internal consideration within Adaptec -- carried over

Larry Barnes to provide access information for the LSI transceiver models to the web site.

Status: Model is available internally within LSI Logic and will be made available to T10 web site as soon as the internal LSI web site is on line -- carried over

Jie Fan, Madison Cable to provide a cable media model to the web site.

Status: model is still under development and will be made available in HSPICE form -- carried over

Bob Gannon to provide a plan to get a model for the transition regions.

Status: plan will be presented at the March 01 meeting

Dean to send emails to all folks with open action items on Tuesday of each week (until the action item is completed).

Status: done - action item will be retained for all meetings if any open action items exist.

Ham to post the draft minutes of the March 01 meeting after review by Dean and the approved minutes of the December meeting.

Status: done

Larry Barnes to supply component definition and a graphical representation for the backplane (should not contradict the transceiver board if possible)

Status: carried over

## 22.2 New action items from present meeting

Paul Aloisi to provide Don Getty contact info to J. Lohmeyer for the T10 modeling web site.

Status: done

Tariq to provide hotel info for the April meeting in Milpitas ASAP

Status: done

Paul Aloisi to contact Tariq to expedite the April meeting announcement

Status: done

Paul Aloisi to place multidrop cable assemblies on the agenda for the next meeting.

Status: done

Bob Gannon to produce matrix of transition regions and issues with each.

Status: today?? new

Larry Barnes to provide information and techniques to allow generation of an IBIS model. This information will take the form of a section in the SSM document and is expected to be used by SSM folks in creating their transceiver models. This will be part of a rev of the SSM document and is expected to be placed on the T10 web site before the end of May 2000.

Status: new

Dean Wallace to direct an action item to address the methodology for incorporating ISI precompensation into an IBIS model.

Status: new

Tariq to facilitate contact between Adaptec and Bruce Manildi of Seagate to explain the nature and purpose of the IBIS modeling methodologies and its relationship to IP.

Status: new

Hitachi cable to provide cable media models to the SSM web site (per last meeting minutes).

Status: new

Section owners are to create basic material and submit to Larry Barnes before the next meeting.

Status: new and ongoing

## 23. Adjourn

The meeting adjourned at 6:00 PM



