Quantum™
Quantum Corporation
500 McCarthy Boulevard
Milpitas, CA 95035 USA

To: T10 Technical committee
From: Mark Evans
Phone: 408-894-4019
Fax: 408-952-3620
Email: mark.evans@quantum.com
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Subject: Details of test set-up used by Quantum for Ultra320 data

Introduction:

Quantum has performed a significant amount of testing for Ultra320 SCSI on several system configurations comprised of currently available, "off-the-shelf" components. Standard test equipment was used to generate and capture the signals.

This data has been presented to T10 in the following documents: T10/00-147R0, Ultra320 SCSI vs. Ultra160 SCSI Eye Diagram Data by Russ Brown, 22 pp.; T10/00-153R0, Ultra320 SCSI with Receiver Equalization 25 m. into Backplane with 6 loads by Russ Brown, 16 pp.; T10/ 00-154R0, Ultra640 SCSI with Receiver Equalization 25 m. into Backplane with 6 loads by Russ Brown, 11 pp.; T10/00-169R0, Effect of Varying Transmitter Amplitude on Ultra320 SCSI Receiver Equalization by Russ Brown, 11 pp.; and T10/00-195R0, Ultra320 into fully populated 10-slot backplane by Russ Brown, 9 pp., (earlier data without crosstalk and ISI was presented in T10/99-335R0, Transmitter Pre-Compensation for 320 MB/sec SCSI by Andrew Bishop, 78pp.). These documents are available at http:www.t10.org.

In the following, details of all elements of the tests performed by Quantum will be described so that others may duplicate the testing performed by Quantum in order to validate Quantum's testing and to insure correlation of other test data presented to T10. The system components used for this testing were selected because they were available or made available by their manufacturers or their representatives and were considered to be representative of commonly available parallel SCSI components. The selection of these components is not meant to imply an endorsement of those components by Quantum.

Following the system configuration details are the procedure used to set up the worst-case crosstalk and the data pattern used for the testing. A compilation of the pictorial representations and schematic for the test configurations from the previously presented documents may be seen in 00-215r0.ppt.

If additional details about this testing are desired, please contact Mark Evans at the phone number or email address listed above.

For all test configurations:

- A Tektronix AWG2041 with 50 Ω output impedance was used to generate differential data on the pair DB(0)+ and DB(0)- at one end of the cable assemblies

- 400 mV was used for all signals generated without precompensation except where indicated in T10/00-169R0 (400 mV was originally selected so that data for precompensation using up to 1.8× boost could be taken while remaining within the SCSI spec (400 mV × 1.8 = 720 mV < 800 mV)).
- An HP81130A was used to generate differential crosstalk at 50 Ω on the pairs DB(1)+ and DB(1)-, and P1+ and P1-.
- Receiver devices designated with the lowest numbers were closest to the transmitter (e.g., the receiver device designated "bp1" in configuration 3 was the device closest to where the cable connected to the backplane and farthest from the terminator on the backplane, and the device designated "bp6" in configuration 3 was the device farthest from where the cable connected to the backplane and closest to the terminator on the backplane).
- Balanced 100 Ω termination (100 Ω ± 1% resistors) was located at the end of the backplane signal path.
- A Tektronix P6247 1Ghz differential probe was used to measure the signals on DB(0)+ and DB(0)- at the connector of the receiving drive.
- All receiver devices were Quantum Ultra160 hard disk drives with a maximum of 12 pF capacitance on the signal lines.

System Configuration 1:

- 10 meter cable assembly using Madison 28AWG round shielded cable supplied by Amphenol Interconnect (Fast-40 cable assembly, p/n 68SKD00071)
- 6-slot backplane (a SCSI LVD backplane, numbers on the back of the system include PB689984-001, MP698758-001, INSK80700087, PBA 688265-005) fully populated with six Quantum Ultra/160 drives
- A LeCroy DDA 120 was used to capture the data at 4 gigasamples per second

System Configuration 2:

- 2.25 meter cable assembly using Hitachi 32AWG twisted-flat cable supplied by Hitachi & Circuit Assembly
- 6-slot backplane (a SCSI LVD backplane, numbers on the back of the system include PB689984-001, MP698758-001, INSK80700087, PBA 688265-005) fully populated with six Quantum Ultra/160 drives
- A LeCroy DDA 120 was used to capture the data at 4 gigasamples per second

System Configuration 3:

- 10 meter cable assembly using Hitachi SMQT 32AWG twisted-flat cable supplied by Hitachi and Circuit Assembly with nine Quantum Ultra/160 drives installed on the connectors having 25 cm spacing between connectors beginning 7.25 meters from the initiator
- 6-slot backplane (a SCSI LVD backplane, numbers on the back of the system include PB689984-001, MP698758-001, INSK80700087, PBA 688265-005) fully populated with six Quantum Ultra/160 drives
- A LeCroy DDA 120 was used to capture the data at 4 gigasamples per second

System Configuration 4:

- 10 meter cable assembly using Hitachi SMQT 32AWG twisted-flat cable supplied by Hitachi and Circuit Assembly with connectors having 25 cm spacing between connectors beginning 7.25 meters from the initiator (no drives were installed on the cable in this configuration)
- 10-slot backplane (numbers on the back of the system include SP#387067-001, P19470CBFIVBTH, AS#00944-001, DG#00945-00, Rev 0C) fully populated with ten Quantum Ultra/160 drives
- A LeCroy DDA 120 was used to capture the data at 4 gigasamples per second

"25 meter" system configuration:

This configuration was used for testing at both Ultra320 and Ultra640 data transfer rates.

- 25 meter cable assembly using Madison 28AWG round shielded cable supplied by Amphenol Interconnect Products (p/n 50833MIOD)
- 6-slot backplane (a SCSI LVD backplane, numbers on the back of the system include PB689984-001, MP698758-001, INSK80700087, PBA 688265-005) fully populated with six Quantum Ultra/160 drives
- For the test at 320 MB/s: a LeCroy DDA 120 was used to capture the data at 4 gigasamples per second
- For the test at 320 MB/s: a Tektronix TDS694C was used to capture the data at 10 gigasamples per second

Note: Samples of a cable assembly using Madison Universal SCSI cable for Fast-80 and all slower speeds (p/n 68KDK00049), can be obtained from Amphenol Interconnect. We have just received a sample for future tests.

Procedures to setup worst-case cross talk:

1. Drive a "...1010..." pattern on the aggressor lines (DB(1)+, DB(1)-, P1+, and P1-) while driving the victim lines (DB(0)+ and DB(0)-) with the test pattern. The amplitude of the signals on the aggressor lines should be equal to the amplitude of the signals on the victim lines (e.g., for a victim signal using no precompensation, the aggressor signal amplitude should be 400 mV, and for a victim signal using 1.8× precompensation, the aggressor signal amplitude should be 400 mV × 1.8 = 720 mV).
2. Align the P1+ and P1- signals to be within 0.5 ns to 1.5 ns of the DB(0)+ and DB(0)- signals. The crosstalk is worst when the aggressor is aligned close to the zero crossing of the victim line but not perfectly coincident.
3. Turn off the signals driving DB(0)+ and DB(0)- and monitor them with the differential probe. Do not disconnect the source because the source output impedance is the termination of the cable.
4. With phase position of P1+ and P1- fixed and driving, adjust the phase of DB(1)+, DB(1)- until maximum peak signal is obtained on DB(0)+ and DB(0)- lines.
5. Drive DB(0)+ and DB(0)- with the test pattern with both aggressors still running.
6. Data now can be collected for the cross-talk.

Test pattern:

The following is approximately the test pattern used for all configurations. The pattern is 1600 bits long and takes a total of 10 μs to transmit at 80 MHz and 5 μs to transmit at 160 MHz. For 80 MHz: this pattern begins with the signal being negated for 600 ns, followed by the signal being asserted for 200 ns, followed by the signal being negated for 200 ns, followed by 1600 ns of "...1010..." transitions, followed by a pseudo random data pattern, ending with the signal being negated. For 160 MHz the number of bits is the same but the times are halved. The data pattern was constructed to provide a variety of transition lengths and is not completely random because, for example, the chance that a completely random pattern would produce a run of 20 zeroes followed by a one and then a few more zeroes (an isolated pulse) is on the order of ten million to one, whereas this run occurs much more frequently in actual data streams.

BINARY	HEX	BINARY	HEX
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	0 0 1 0 1 1 1 0 1 0 1 1 1 1 1 1	2EBF
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	1 0 1 0 1 1 1 0 0 1 0 0 1 0 1 0	AE4A
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	0 0 1 0 1 1 0 1 1 1 1 0 0 0 0 0	2DE0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	0 0 1 0 1 0 1 0 1 0 0 0 1 0 1 0	2A8A
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	1 0 1 1 1 0 1 0 1 0 1 1 1 1 1 0	BABE
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	1 0 1 0 1 0 0 0 1 0 1 0 0 0 1 0	A8A2
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	FFFF	1 1 1 1 0 0 1 0 1 0 1 1 1 0 1 0	F2BA
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	FFFF	1 0 1 1 1 0 1 0 0 0 0 1 1 0 1 0	BA1A
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	1 0 1 1 1 0 1 0 1 0 1 0 1 1 1 0	BAAE
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	0 1 0 0 0 1 1 0 0 1 0 0 0 0 1 0	4644
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0	0300
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1	7FE7
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	1 1 1 1 1 1 1 0 0 0 0 0 1 1 1 0	FE0E
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0	01FE
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 0 1 1 1 1 1 1 1 1 0 0 0 0 0 0	34C0
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	1 0 0 0 0 1 1 1 1 1 1 0 1 1 1 1	87CF
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 0 0 1 1 0 0 1 1 1 0 1 0 0 1 1	19D3
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 1 0 1 0 1 1 1 0 0 1 0 0 1 0 1	5725
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 0 0 1 0 1 1 0 1 1 0 0 0 0 0 0	16C0
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 0 0 0 0 0 0 1 0 0 0 0 1 1 1 1	010F
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	1 1 0 1 1 1 1 0 0 0 1 1 0 0 1 1	DE33
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	1 0 1 0 0 1 1 0 1 0 1 0 1 1 1 0	A6AE
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 1 0 0 1 0 1 0 0 0 1 0 1 1 0 1	4A2D
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	1 0 0 0 0 0 0 1 1 1 1 1 1 0 1 1	81FB
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	1 1 0 0 0 0 0 0 1 0 0 0 0 1 1 1	C087
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	AAAA	0 0 1 1 0 0 0 1 0 1 1 0 0 1 0 1	3165
1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 1	CCCD	0 1 0 1 0 0 0 1 1 0 1 1 0 1 0 1	51B5
1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 0	E1E0	1 1 0 1 0 0 1 0 0 1 1 1 1 1 1 1	D27F
1 1 1 1 1 0 0 0 0 0 1 1 1 1 1 0	F83E	1 0 0 0 0 0 0 0 1 1 0 1 0 1 0 0	80D4
0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 1 1	07EB	0 0 0 1 0 0 1 1 0 0 1 1 0 1 1 1	1337
1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 0	FC02	0 1 1 0 1 0 0 0 0 1 0 0 0 1 1 1	6867
0 0 0 1 1 1 1 1 1 0 1 1 1 1 0 0	1FBC	1 1 1 0 0 0 1 1 1 0 0 0 1 0 0 1	E389
0 1 1 0 0 1 1 1 0 1 0 0 1 1 0 1	674D	1 0 0 0 0 1 0 1 1 0 0 0 0 1 0 1	8585
0 1 0 1 1 1 0 0 1 0 0 1 0 1 0 0	5C94	1 1 0 1 0 1 1 1 1 1 1 1 0 1 1 0	D7F6
0 1 0 1 1 0 1 1 0 0 0 0 0 0 0 0	5B00	0 0 1 1 0 0 1 1 0 0 0 0 1 0 1 1	330B
0 0 0 0 0 1 0 0 0 0 1 1 1 1 1 1	043F	1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	BFFF
0 1 1 1 1 0 0 0 1 1 0 0 1 1 1 0	78CE	1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1	FEFF
1 0 0 1 1 0 1 0 1 0 1 1 1 0 0 1	9AB9	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	FFFF
0 0 1 0 1 0 0 0 1 0 1 1 0 1 1 0	28B6	0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 1	0E01
0 0 0 0 0 1 1 1 1 1 1 0 1 1 1 1	07EF	0 0 0 0 1 1 1 1 1 1 0 1 1 1 1 0	0FDD
0 0 0 0 0 0 1 0 0 0 0 1 1 1 0 0	021C	0 0 1 1 0 0 1 1 1 0 1 0 0 1 1 0	33A6
1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	C595	1 0 1 0 1 1 1 0 0 1 0 0 1 0 1 0	AE6A
0 1 0 0 0 1 1 0 1 1 0 1 0 1 1 1	46D7	0 0 1 0 1 1 0 1 1 0 0 0 0 0 0 0	2D80
0 1 0 0 1 0 0 1 1 1 1 1 1 1 1 0	49FE	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000
0 0 0 0 0 0 1 1 0 1 0 1 0 0 0 0	0350	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	8000
0 1 0 0 1 1 0 0 1 1 0 1 1 1 0 1	4CDD	1 1 1 0 1 0 1 1 1 0 0 1 0 0 1 0	EB92
1 0 1 0 0 0 0 1 0 0 0 1 1 1 1 1	A11F	1 0 0 0 1 0 1 1 0 1 1 1 1 0 0 0	8B78
1 0 0 0 1 1 1 0 0 0 1 0 0 1 1 0	8E26	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000
0 0 0 1 0 1 1 1 0 1 0 1 1 1 1 1	175F	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000
1 1 0 1 1 0 0 0 1 1 0 0 1 1 0 0	D8CC	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000