T10 physical test study group 00-178r0
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1. Introduction

The T10 physical test study group meeting was called to ensure that T10 members know what is going on within T10 and the rest of the industry that relates to physical test of signals and components. This study group meeting may be a one time event and is not necessarily expected to continue. An expected outcome of this meeting is to identify specific holes in the testing efforts for T10 interests that may need additional attention. This additional attention may be implemented by creating yet more working groups or (preferably) by adding to the work content of the groups that are already established.

2. Background

This document is intended to describe the work going on that relates directly or indirectly to physical test of SCSI signals and the components that produce, carry, influence, or detect these signals.

There are six formal efforts underway in the industry at the moment that are specifically aimed at the general problem of specification and verification through testing of signals used to transport storage data. These efforts indirectly affect component design as well. Two of these are directly under T10, two are under SFF, and two are under T11. Another effort was recently completed for SCSI cable media and the results are contained in SPI-3.

Specifically the efforts are:

- SCSI passive interconnect performance (SPIP) (T10 working group)
- SCSI signal modeling (SSM) (T10 working group)
- High speed serial duplex (and parallel serial) copper performance and testing (HDCI) (SFF project)
- FC signal modeling (no acronym yet) (T11 working group)
- Methodologies for jitter specification -2 (MJS-2) (T11 working group)

- High speed optical interconnect performance (HSOI) (SFF project)

All six are using the basic methodology established in the HDCI group over the last three years. This methodology consists of three key parts:

1. Dividing all tests into two basic types:

- (level 1) those required to ensure the performance of the component under system operating conditions
- (level 2) those that may be required to diagnose or characterize parameters that effect the level 1 test results

2. Requiring performance specifications and test conditions to be at the most extreme allowed which includes:

- ensuring that all legal noise sources are present when executing the tests
- ensuring that the test fixture effects do not compensate for degradations in the components under test
- adjusting the performance requirements so that the effects of the worst case allowed launch signals are accounted for when using signals from real equipment
- accounting for resonance and frequency dependent effects that may be present

  In addition, the following two features are under development from the modeling efforts:

  - using modeling where needed to account for effects of practical testing disturbances
  - specific methods for validating modeling results through practical measurement

3. Using a structured approach where the test processes are rigorously specified through the following steps:

- general description
- test equipment requirements
- test equipment calibration
- test fixture requirements
- test fixture calibration
- test environment calibration
- test execution
- data output format
- allowed values for valid test
- [allowed performance levels – either by reference or by direct inclusion]

3. Specific work content from each group identified above

A brief description of each of these efforts follows.

3.1 SCSI passive interconnect performance (SPIP) (T10 working group)

This group is in the process of producing a committee document that contains the work described below.

The following is a list of goals for SPIP:

- Focused on the cable assembly/backplane as a finished component including all connectors and transition regions.
- May be either internal or external.
- Define how to specify the output signal from a cable assembly in light of the possible use of adaptive filtering (called equalization by some) in receivers.
- Allow for the following schemes that are presently being considered for SPI-4: transmitter compensation, adaptive filtering, compensation of skew
- Define how to specify cable assembly construction in terms of performance rather than only in mechanical terms. For example, connector to connector spacing in terms of propagation time rather than length, transition regions in terms of cross talk contribution rather than physical extent, discontinuities in impedance due to connectors rather than nothing, etc.
- Preserve the present testing methodologies for media if possible.
- For example, the attenuation test can be generalized to two port amplitude transfer function (which will include resonance caused by connectors etc). The cross talk test can be generalized by using repeated pulses and varying the rep rate while observing the response of on the victim line.
- Recognize that the effects of data pattern and placement of cable assembly features may produce complex interference patterns and recommend how to minimize the impact of these features on the delivered signal.
- Use the same test specification methodology as used for SPI-3 cable media.
- Add common mode requirements to the cable assembly tests (both shielded and unshielded)

3.2 SCSI signal modeling (SSM) (T10 working group)

The output of this group is contained in a T10 technical report under development.

The following is the present SSM document outline with the names of some of the responsible folks:

1. SCOPE ((Larry Barnes - 100%)
2. REFERENCES
2.1 Approved references
2.1.1 References under development
2.2 Resources
2.2.1 Publications (Jonathan Fasig - 100%)
2.2.2 Online bookstores & publishers - deleted for legal reasons
2.2.3 Other online resources - deleted for legal reasons
2.3 Tools (group - 80%)
3. DEFINITIONS, ACRONYMS, SYMBOLS, KEYWORDS, AND CONVENTIONS (group)
3.1 Definitions (20%)
3.2 Acronyms (80%)
3.3 Symbols and Abbreviations (100%)
3.4 Keywords (100%)
3.5 Conventions (100%)
4.0 Overview (Bill Ham - 25%)
6. MODELS
6.1 General recommendations (Larry Barnes - 10%)
6.1.1 Supporting documentation
6.1.2 Behavioral models
6.1.3 Circuit Models
6.2 Cables
6.2.1 Cable media (bulk cable) (Jie Fan / Zane Daggett - 10%)
6.2.2 Transition region (Bob Gannon, Greg Vaupotic - 10%)
6.3 Connectors (Martin O. - 5%)
6.3.1 Cable connectors
6.3.2 Non-cable connectors
6.3.2.1 RLC transmission line matrix
6.4 Printed circuit boards (Matt S., Tariq A. - 30%)
6.4.1 Traces
6.4.1.1 Microstrip
6.4.1.2 Stripline
6.4.1.3 Broad coupled stripline
6.4.1.4 Offset broad coupled stripline
6.4.2 Discontinuities
6.4.2.1 Vias
6.4.2.2 Pads
6.5 Devices
6.5.1 Terminators (Paul Aloisi / Don Getty - ?)
6.5.2 Transceivers (Dean Wallace - 5%)
6.5.3 Packages (Larry Barnes - 5%)
7. STANDARD MODEL CONSTRUCTIONS
7.1 Host bus adapter / target board (Tariq / Matt S. - 70%)
7.2 Point to point cable assemblies (Dima Smolyansky - 40%)
7.3 Multidrop cable assemblies (TBD)
7.4 Backplane (Larry Barnes - 10%)
7.5 System model (group - 2%)
8. VALIDATION PROCEDURES
8.1 Physical measurement points (Greg Vaupotic - ?)
8.2 Access to measurement points (Larry Barnes / Martin O.)
8.2.1 device connector
8.2.2 chip to board interface
8.2.3 terminator connector
8.3 Instrumentation input models (Jason Chou - 5%)
8.3.1 scope probe models
8.3.2 network analyzer models

8.3.3 test port cables
8.3.4 instrument transfer function
8.4 Use of frequency / time domain for validating elements of component models (
8.5 Distributed vs lumped resonance issues
8.6 Behavioral
8.7 Circuit
9. SIMULATION INTEGRATION STRATEGY (Dean Wallace)
9.1 System configurations
9.2 Data patterns
9.3 Data rates

3.3 High speed serial duplex (and parallel serial) copper performance and testing (HDCI) (SFF project)

This group has produced the basic document: SFF 8410 rev 16 whose outline follows:

1. Introduction 16
2. General 16
3. High frequency performance requirements 20
3.1 HSS test levels 20
3.1.1 Level 1 test definition 20
3.1.2 Level 2 test definition 21
3.1.3 Relationship between level 1 and level 2 tests 21
3.2 Applicability to specific connectors 22
3.3 Electrical Neighborhood 22
3.4 Definition of level 1 HSS electrical performance parameters 24
3.4.1 Definition of PUT and PUTNOT 24
3.4.2 Definition of level 1 electrical performance parameters 26
3.5 Definition of level 2 HSS electrical performance parameters 27
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3.7 Definition of the HSS interconnect under test (IUT) 29
3.8 Special considerations for test fixtures 30
3.9 Extensions to parallel - serial constructions 31
3.9.1 Impedance profile for p-s constructions 32
3.9.2 Signal degradation for p-s constructions 32
3.9.3 Balance degradation for p-s constructions 33
3.9.4 EMC for p-s constructions 33
3.9.5 Near end cross talk for p-s constructions 33
3.9.6 Summary of extensions to p-s constructions 34
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4.1.2.3 Differential signal transition duration calibration 37
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4.1.3.1 Impedance profile in connector region 40
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4.5.4 Acceptable ranges 79
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5.1 Attenuation 80
5.1.1 Measurement test fixture and measurement equipment 85
5.1.2 Calibration procedure 87
5.1.3 Testing procedure 87
5.1.4 Acceptable ranges 89
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5.2.1 Test fixture and measurement equipment 89
5.2.2 Calibration procedure 90
5.2.3 Testing procedure 91
5.2.4 Acceptable ranges 92
5.3 Amplitude imbalance between the + signal and - signal 92
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5.3.2 Calibration procedure 93
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6.4 EMC 105
6.5 NEXT (Quiescent noise) 105

3.4 FC signal modeling (no acronym yet) (T11 working group)

This group is expected to produce a technical report. There is no specific output yet available as this is a very new effort.

3.5 Methodologies for jitter specification -2 (MJS-2) (T11 working group)

Following is the presently agreed organization of the MJS-2 document with names of those responsible for specific sections:

Sections 1 thru 5 - Ham

1. Introduction
1.1. Document scope and purpose
1.2. Document organization
2. T11.2 Membership
3. References
4. Definitions and conventions
4.1. Conventions
4.2. Acronyms
4.3. Definitions
5. Scope
5.1. Motivation and goals
5.2. Authority
6. Jitter overview
6.1. FC-0 and MJS (-1) interface overview - Ham
6.2. Fibre channel storage implementation - copy if possible
6.3. Jitter contribution elements - Wavecrest Mike Li
6.3.1. Reference times - TBD
6.3.2. Signal amplitude effects - TBD
6.3.3. Generalized jitter concepts - TBD
6.3.4. Deterministic contributors (copy)

6.3.5. Random contributors (copy)
6.4. Improved Bit Error Rate vs. Jitter Model (copy from MJS-1) - Tom Lindsay if mods needed
6.4.1. Description of Mathematical Model
6.4.2. Random Jitter
6.4.3. Addition of Deterministic Jitter
6.5. Equalization - Mike Jenkins
6.5.1. Filtering
6.5.2. Pre-emphasis
6.5.3. Adaptive transmitters
6.5.4. Adaptive receivers
6.5.5. Distributed

6.6. Separation of jitter components - Tom Lindsay
6.6.1. Need to separate components
6.6.2. General considerations
6.6.3. Mathematical basis
6.6.4. Accuracy and precision
6.6.5. Tools
6.7. Jitter accumulation and transfer- Tom Lindsay
6.8. Data rate considerations
6.9. Effects of parallel paths - skew, cross talk, imbalance
6.10. Pattern dependent random jitter - Mike Jenkins
6.11. Jitter methodologies (copy from MJS if relevant)
6.11.1. Current practice and specifications
6.11.2. Jitter measurement definitions
7. Jitter test methodologies - Ham
7.1. Goals - Ham
7.2. Level 1 and level 2 tests - Ham
7.3. System considerations - TBD
7.4. Component considerations - TBD
7.5. Instrumentation considerations - TBD
7.5.1. LESB
7.5.2. BER
7.5.3. FC compliant
7.5.4. Non-FC compliant
7.5.5. Built in test features
7.6. Test fixture considerations - Ham
7.7. System / environmental noise considerations
7.8. Reference standards / calibration considerations
7.9. Data output format considerations
7.10. Jitter output test methodologies (copy from MJS)
(need effect of high pass filter discussion)
7.10. Jitter tolerance test methodologies (copy from MJS)
(need reference to jitter output section for tolerance test conditions)
8. Requirements for specific tests
[Only one example is shown for simplicity – need to generate a comprehensive list – this will be a very long section]
8.1. Optical Gamma T output (started already)
8.1.1. FC device (requires full protocol signals to work) - Rich Feldman (Bert and scope methods only)
8.1.1.1. Overview
8.1.1.2. Test Fixtures
8.1.1.3. Instrumentation
8.1.1.4. Calibration
8.1.1.5. Test execution
8.1.1.6. Data output formats
8.1.1.7. Acceptable values
8.1.2. FC protocol neutral component - TBD
8.1.2.1. Overview
8.1.2.2. Test Fixtures
8.1.2.3. Instrumentation
8.1.2.4. Calibration
8.1.2.5. Test execution
8.1.2.6. Data output formats
8.1.2.7. Acceptable values
8.2. Copper Gamma R output
8.2.1. FC device transmitter (requires full protocol signals to work) - TBD
8.2.1.1. Overview
8.2.1.2. Test Fixtures
8.2.1.3. Instrumentation

8.2.1.4. Calibration
8.2.1.5. Test execution
8.2.1.6. Data output formats
8.2.1.7. Acceptable values
8.2.2. FC protocol neutral component - TBD
8.2.2.1. Overview
8.2.2.2. Test Fixtures
8.2.2.3. Instrumentation
8.2.2.4. Calibration
8.2.2.5. Test execution
8.2.2.6. Data output formats
8.2.2.7. Acceptable values
8.3. Copper Beta R tolerance (already started)
8.3.1. FC device (requires full protocol signals to work) - Allen Kramer
8.3.1.1. Overview
8.3.1.2. Test Fixtures
8.3.1.3. Instrumentation
8.3.1.4. Calibration
8.3.1.5. Text execution
8.3.1.6. Data output formats
8.3.1.7. Acceptable values
8.4. Optical Gamma R tolerance - Tom Lindsay
8.4.1. FC device (requires full protocol signals to work)
8.4.1.1. Overview
8.4.1.2. Test Fixtures
8.4.1.3. Instrumentation
8.4.1.4. Calibration
8.4.1.5. Text execution
8.4.1.6. Data output formats
8.4.1.7. Acceptable values
8.4.2. FC protocol neutral component
8.4.2.1. Overview
8.4.2.2. Test Fixtures
8.4.2.3. Instrumentation
8.4.2.4. Calibration
8.4.2.5. Test execution
8.4.2.6. Data output formats
8.4.2.7. Acceptable values
Further sections will be added to section 8 for all interoperability points and all versions - these sections will re-use major parts of the above sections
9. 10 Examples
9.1. Jitter budget allocations - TBD
9.2. Jitter tolerance specification - TBD
9.3. Revised jitter output allocation tables - TBD
9.4. Separation of jitter components - Dennis Petrich
9.5. Jitter accumulation (+ or-) - Mike Jenkins
9.6. Amplitude to phase conversion - TBD
9.7. Proper use of eye diagrams and masks - TBD

Annex A - Implementation strategies - TBD

A.1 Repeaters
A.2 Latency
A.3 Bandwidth

[These following annexes are extracted from MJS-1 for reference – need to consider what we need for MJS-2.]

Annex B

Improved Test Bit Sequences
B.1 Test bit sequence characteristics
B.1.1 Low Frequency Pattern
B.1.2 Low transition density patterns
B.1.2.1 Half-rate square pattern
B.1.2.2 Quarter-rate square pattern
B.1.2.3 Ten contiguous runs of 3
B.1.3 Composite patterns
B.2 Compliant jitter test bit sequences
B.2.1 Random test bit sequence
B.2.1.1 Background - fibre channel frame
B.2.1.2 Original RPAT
B.2.1.3 Compliant RPAT (CRPAT)
B.2.2 Compliant Receive Jitter Test Bit Sequence
B.2.2.1 Receive Jitter Tolerance Pattern
B.2.2.2 Compliant Receive Jitter Tolerance Pattern
B.2.3 Supply Noise Test Bit Sequences
B.2.3.1 Supply Noise SPAT
B.2.3.2 Supply Noise CSPAT
B.3 System Jitter Testing Issues
Annex C
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C.1 Calibration of a Signal Source using the BERT Scan Technique
C.2 Sinusoidal Jitter Modulation
C.3 Direct Time Synthesis
Annex D
Jitter Output Test Methodologies
D.1 Jitter Output Test Methodologies
D.2 Time Domain Measurement - Scope and BERT Scan
D.2.1 Overview
D.2.2 Golden PLL
D.2.3 Time Domain Scope Measurement
D.2.4 BERT Scan
D.3 Time Interval Analysis
D.3.1 Introduction
D.3.2 "Clock-less" Jitter Measurement
D.3.3 TIA Data Reduction Procedure
D.3.4 Total Jitter Calculation
D.3.5 Power Density Spectrum of Jitter
D.3.6 Data Dependent (ISI) Jitter Measurement
D.3.7 Jitter Measurements with a "Pattern Marker and known pattern"
D.3.8 Jitter Measurement Using a Sampling Oscilloscope (DDJ and PWD)
D.4 Frequency Domain Measurement (Spectrum Analyzer)
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E.2 Basic architecture
E.3 Instrumentation interface adapters
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E.3.1.1 Source and sink adapters for balanced copper variants
E.3.1.1.1 Balanced-unbalanced
E.3.1.1.2 Balanced - balanced (alternative 1)
E.3.1.1.3 Balanced - balanced (alternative 2)
E.3.1.2 Tap adapters for balanced copper variants
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E.3.2.1 Source and sink adapters for unbalanced copper variants (alternative 1)
E.3.2.2 Source and sink adapters for unbalanced copper variants (alternative 2)
E.3.2.3 Tap adapters for unbalanced copper variants (alternative 1)
E.3.2.4 Tap adapters for unbalanced copper variants (alternative 2)
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E.3.3.1 Source interface adapters
E.3.3.2 Sink interface adapter
E.3.3.3 Optical tap
E.3.4 Specific tests
E.3.5 Description of baluns
E.3.5.1 Balun requirements
E.3.5.1.1 Core and transmission-line requirements
E.3.5.2 Specific wound core construction details
E.3.5.2.1 Alternative 1 - wound toroid construction
E.3.5.2.2 Alternative 2 - wound toroid construction
E.3.5.2.3 Alternative 3 - wound bead construction
E.3.5.3 Connection of wound cores into baluns
E.3.5.4 Other source/sink adapter components
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F.2 Elements contributing to jitter
F.3 Hubs
F.4 Retiming hubs
F.5 Repeating hubs
Annex G
Choosing the Corner Frequency: fc / 1 667

3.6 High speed optical interconnect performance (HSOI) (SFF project)

Following is the outline of the optical test document SFF 8412

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2. General 16
2.1 Definition of HSS 16
2.2 Basic unit under test 17
2.3 General requirements 17
2.4 Risks and calibration strategy 18
2.4.1 Signal source characterization and calibration 18
2.4.2 High frequency noise and filtering 20
2.4.3 Test fixture compensation and calibration issues 20
2.4.4 Summary 22
3. Definitions and abbreviations 22
4. High frequency performance requirements 22
4.1 HSS test levels 23
4.1.1 Level 1 test definition 23
4.1.2 Level 2 test definition 23
4.1.3 Relationship between level 1 and level 2 tests 23
4.2 Applicability to specific connectors 24
4.3 Optical signal neighborhood 25
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