Pre-Emphasis Experimental Data

SPI-4 Working Group

Dallas, TX

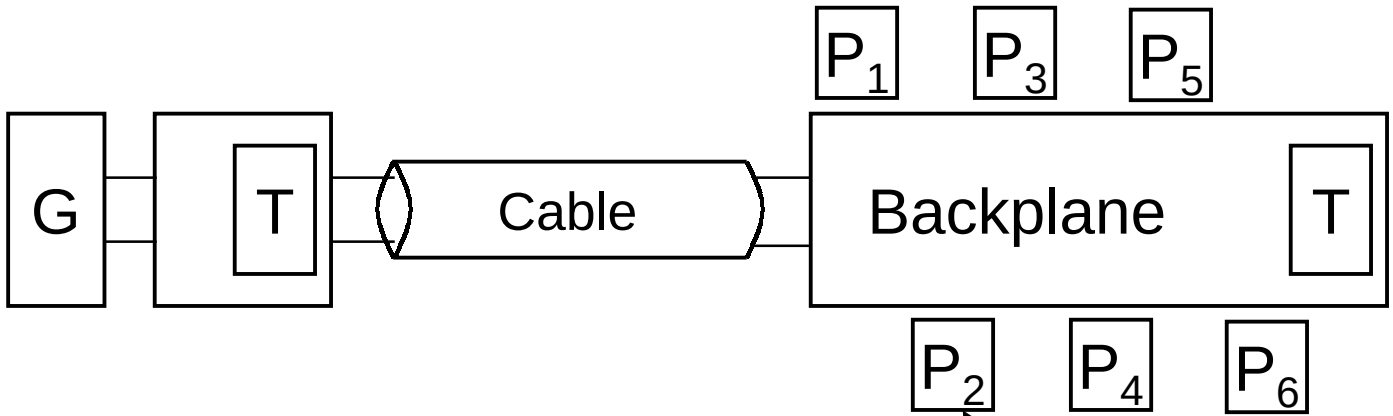
Frank Gasparik

LSI Logic Corporation

Pre-Emphasis Experiment

- System schematic / description
- Cable only, data at 40, 80 and 160MHz
- Loaded system schematic
- Input data pattern
- 80MHz data without Tx boost
- 80MHz data with Tx boost
- 160MHz data without Tx boost
- 160MHz data with Tx boost

Measurement Setup



G ... HP11110A Current Generator

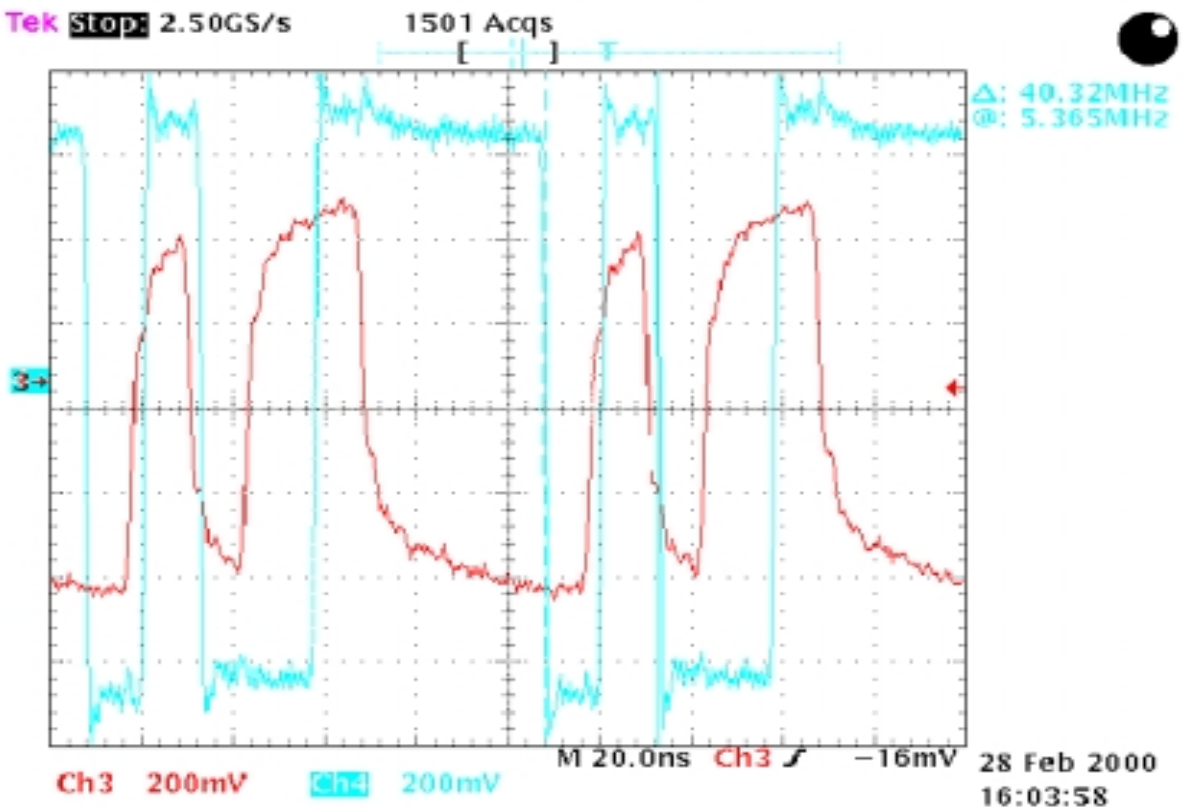
T ... Symmetric 100Ω Termination

Cable ... 10m 28AWG SCSI Round Cable

P_i ... HDD

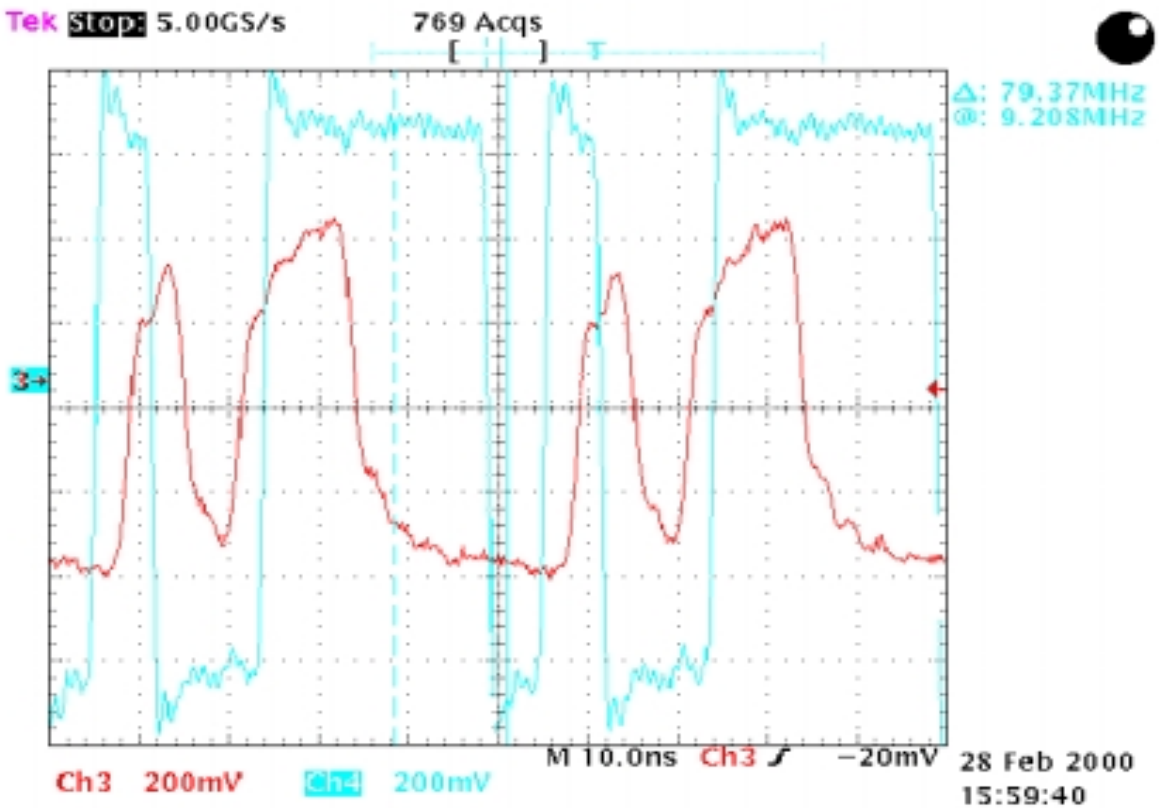
LSI LOGIC

25m Round Cable only @ 40MHz



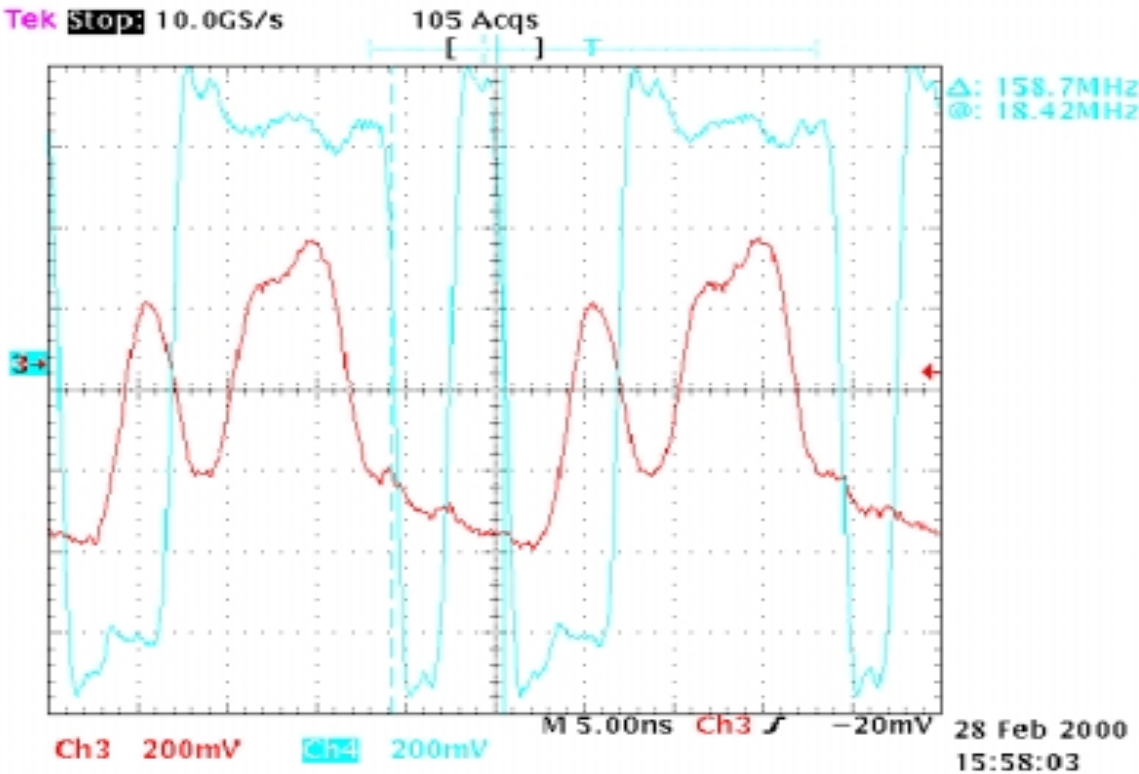
No Boost

25m Round Cable only @ 80MHz



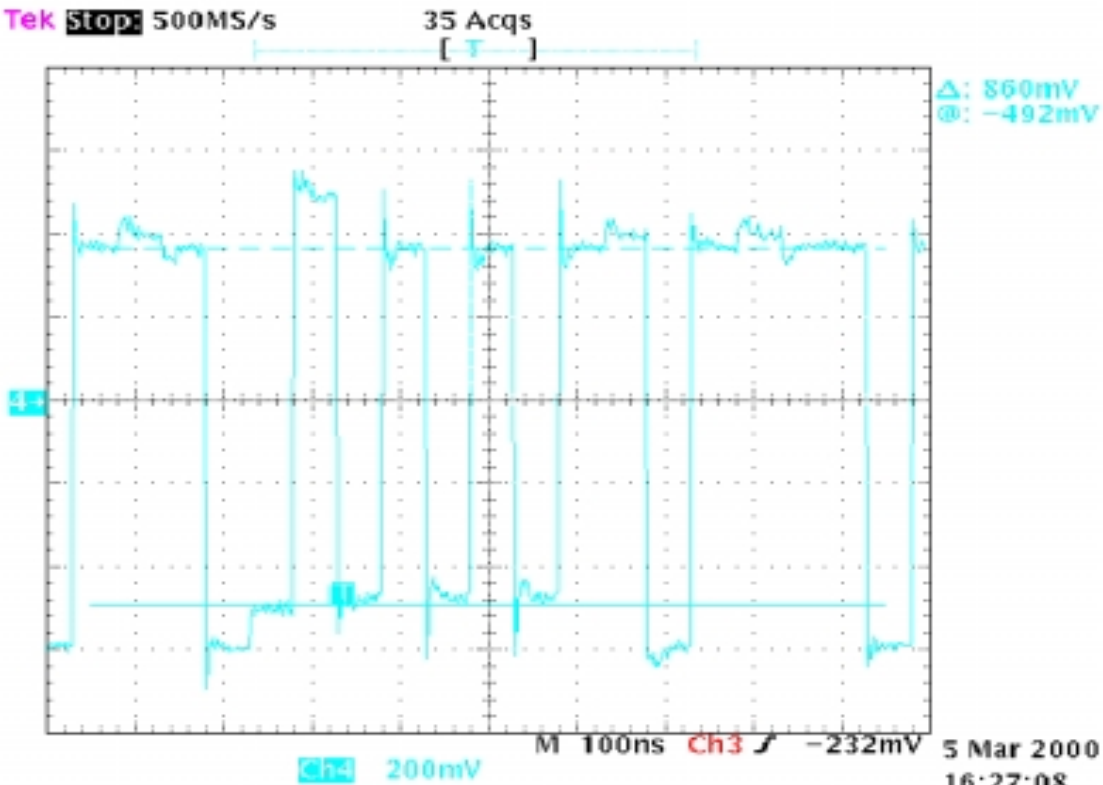
No Boost

25m Round Cable only @ 160MHz



No Boost

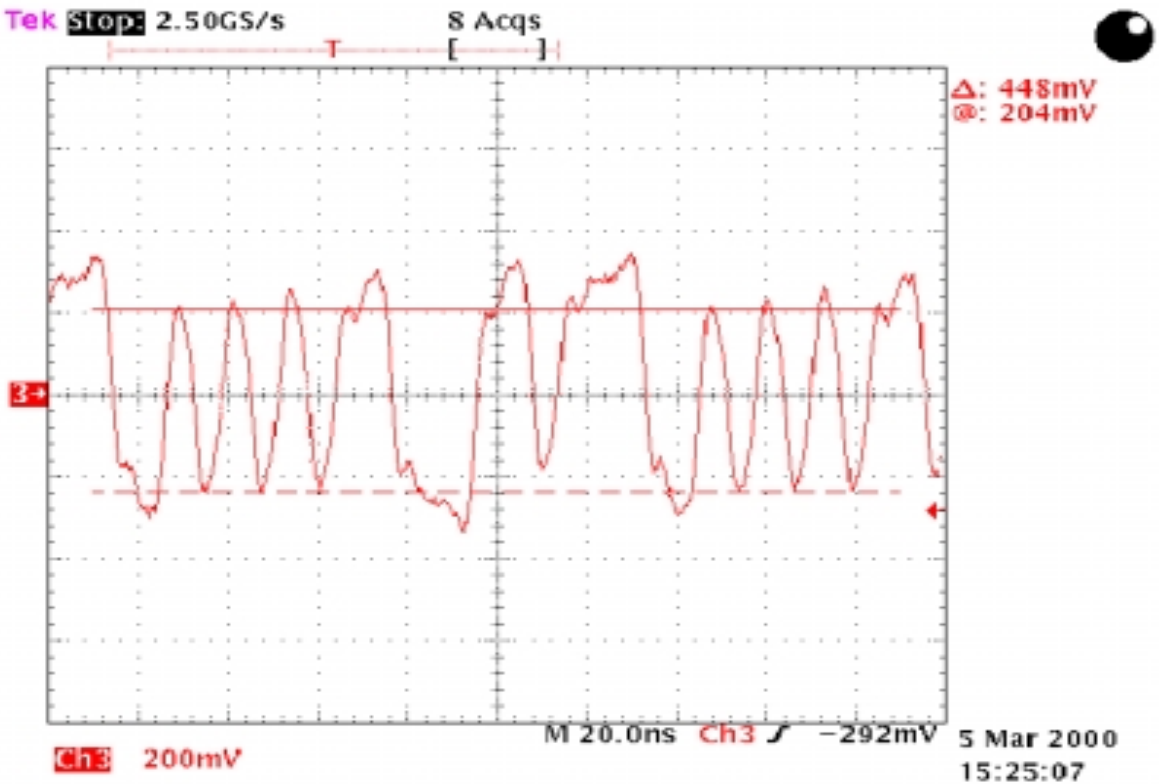
Input Signal Format at 20% Boost



Nominal level 0.86V_{pp}

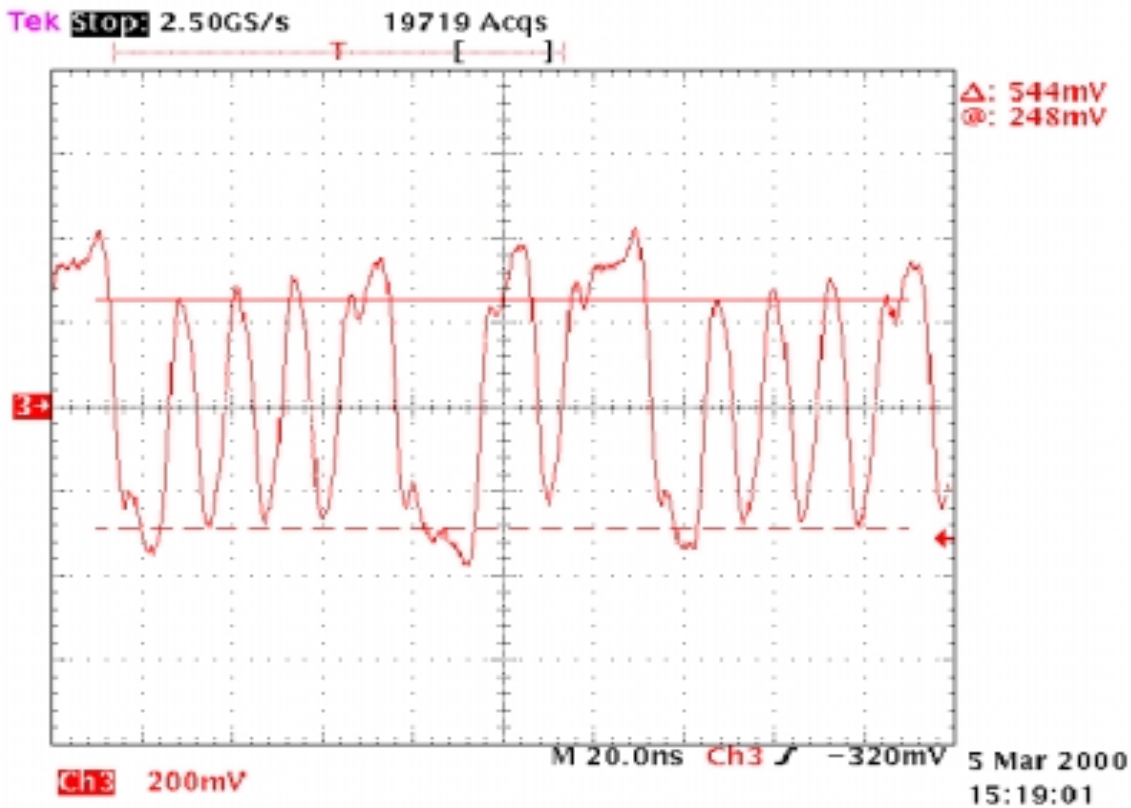
Boost level 1.03V_{pp}

Loaded System @ 80MHz



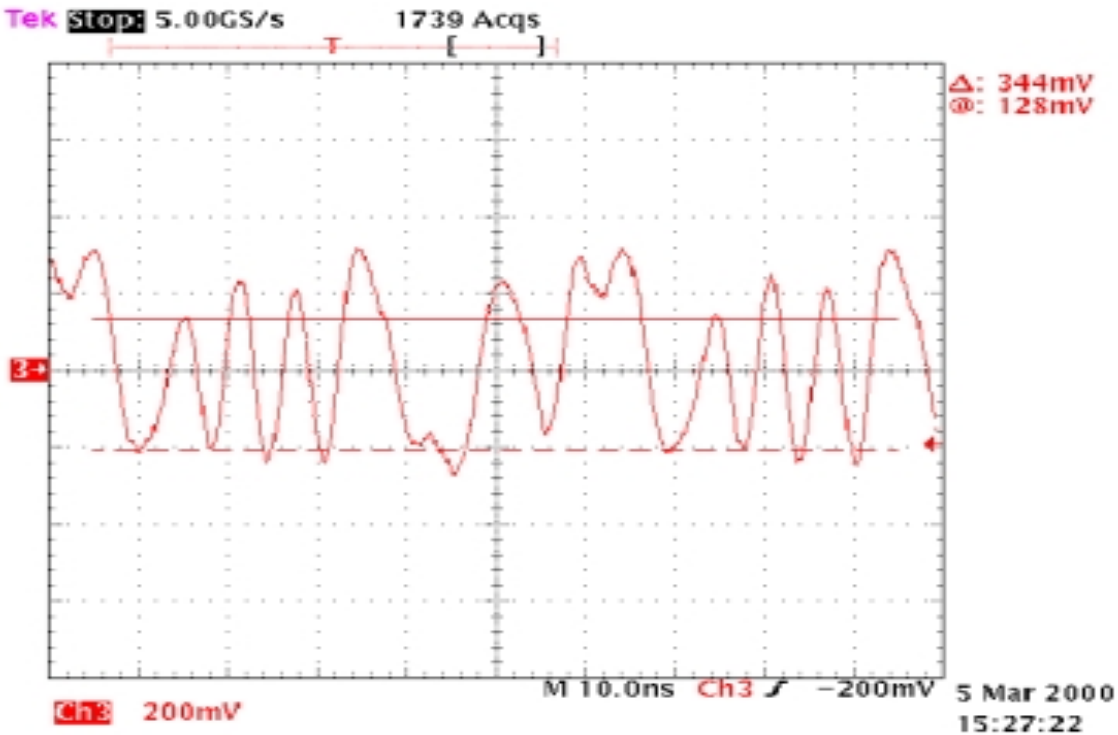
No Boost

Loaded System @ 80MHz



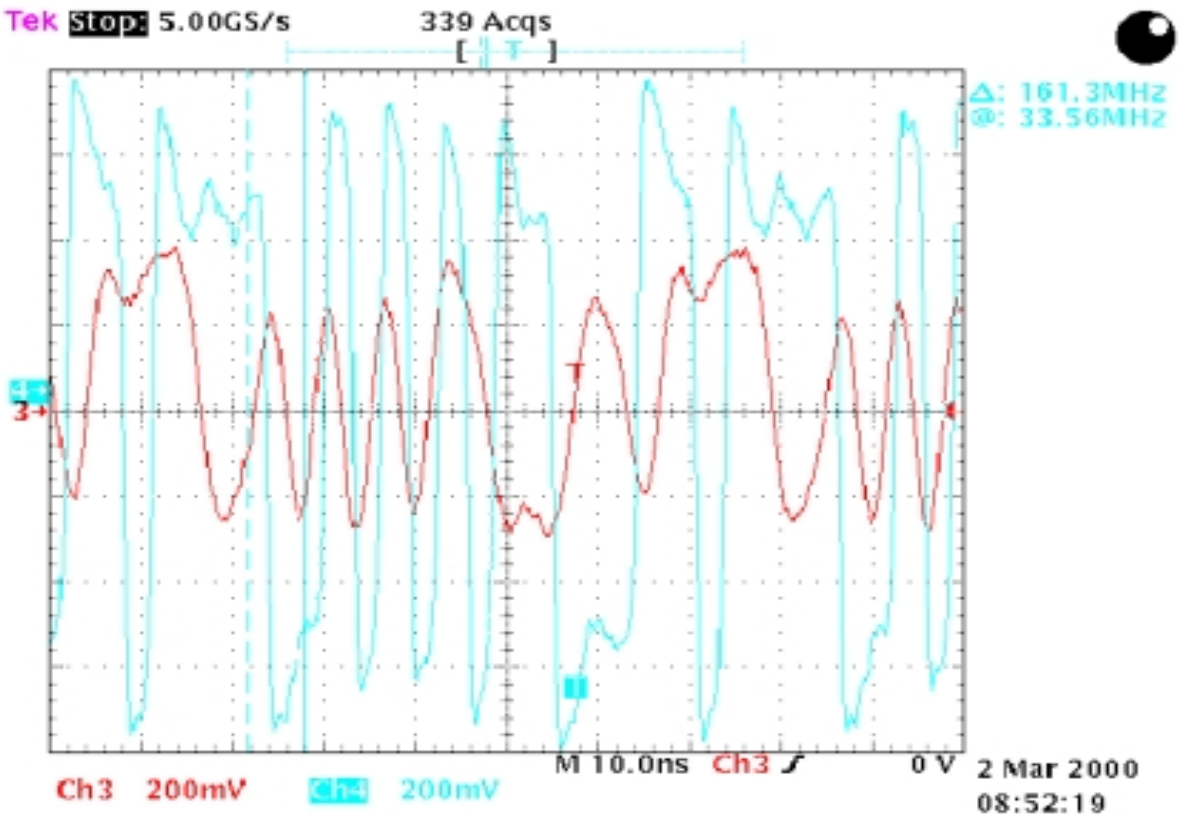
20% Boost

Loaded System @ 160MHz



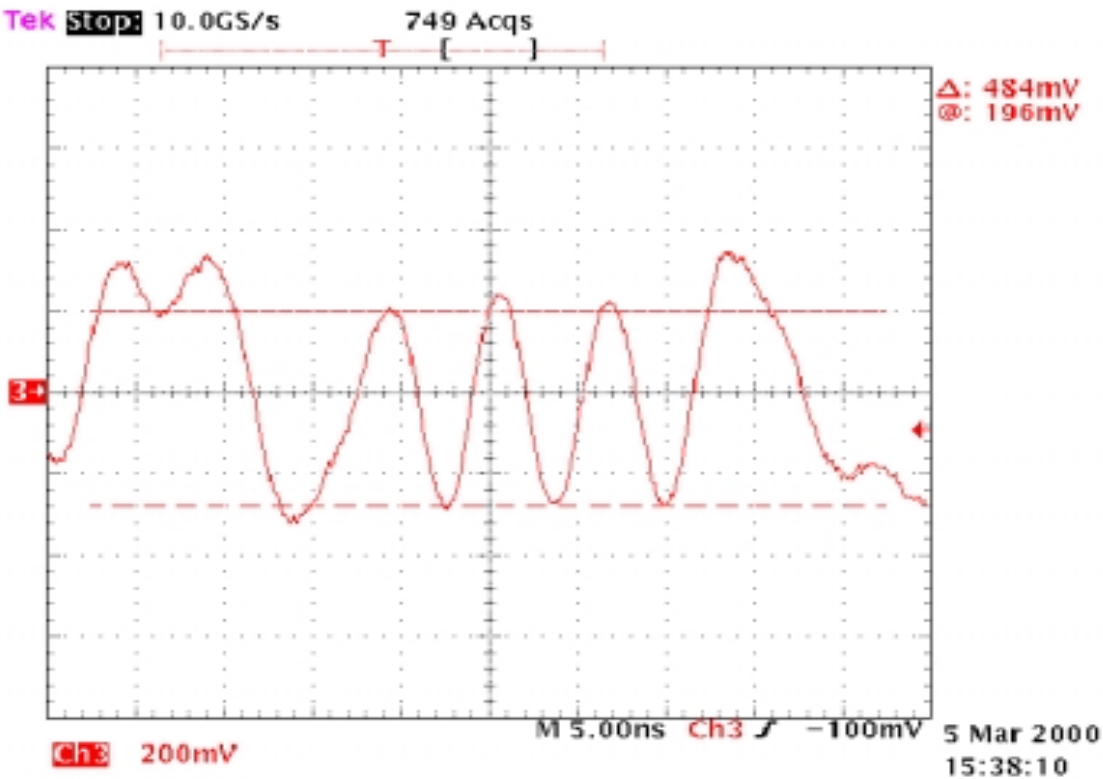
No Boost

Loaded System @ 160MHz



10% Boost

Loaded System @ 160MHz



20% Boost

Pre-Comp Issues and Perspectives

- Common-Mode Issues
- Pre-Comp versus Equalization
- Pad Capacitance
- Slew Rate
- Thermal Issues
- Back Plane Impedance
- Pre-Comp Levels and Algorithms
- Other Options

Common-Mode Issues

- Existing LVD current drivers can't be ideal. All exhibit non-symmetry of signal levels (difference between the I_P and I_N currents)
- Expected pre-comp boost factor is 20% to 30% - not as assumed 50% to 80%
- Pre-compensation needed only after $n \geq 2$ vacant transitions (average I_{CM} will be proportionally smaller)
- EMI should be checked

Pre-Comp versus Equalization

- Tx pre-comp additional driver size and control circuitry estimated as < 5% of LVD/SE pad
- Equalizer die area not free
- Cell size of 3-pole equalizer, including adaptive circuitry is estimated much larger than 5% of pad
- Domain validation already requires controllable, programmable drive levels

Capacitance and SR Issues

- SPI-4 will be designed in the next generation of CMOS technology (smaller driver device junction capacitance)
- Controlled Slew Rates (the driver's $\delta i/\delta t$) in SPI-4 and next generations SCSI is a given requirement
- Optimum adjustable Slew Rate for various load conditions - a desirable feature in the domain validation?

Thermal Issues

- Cross coupled input devices of the LVD differential receiver should eliminate or substantially reduce the chip edge thermal gradient problem
- LVD driver temperature has only secondary effect on the current mirror referenced by the central bias generator

Back Plane Impedance

- Backward compatibility of the SPI-4 systems, working with the marginal SPI-2 and SPI-3 backplanes can’t be supported
- Better backplane designs are not just an option, but a requirement for the SPI-4

Pre-Comp Implementation

- Initial proposal for the pre-comp level is 20% to 30% for Tx signal boost
- Determination of the pre-compensation algorithm (n>3?)

Other Options

- Other forms of filtering
- Test chips for determination of the ideal selection
- More SCSI systems evaluation (eye diagrams, load combinations, data patterns, etc.)
- Complete system modeling and simulations