SCSI HISTORY AND SIGNAL INTEGRITY STRATEGIES

- THE FOLLOWING THREE SLIDES WERE PRESENTED TO THE SCSI SIGNAL MODELING GROUP ON FEBRUARY 08, 2000
- THIS INFORMATION IS PART OF ORIENTING SSM WITH RESPECT TO OTHER ACTIVITIES

BILL HAM
COMPAQ COMPUTER CORP

SCSI HISTORY AND TERMINOLOGY

(BOLD INDICATES PREFERRED NOMENCLATURE-
NOTE THAT TYPE OF CONTENT IS DIFFERENT - READ THE DETAILS)

- **SCSI-1**: (ASYNC SE) ~1.5 MB/SEC (N) 1985 (FULL PROTOCOL + PHYSICAL)
- SCSI-2 :(**SLOW** SE*) 5 MB/SEC (N) 1989 (FULL PROTOCOL + PHYSICAL)
- SCSI-3 DOCUMENT SET:
  - SPI-1 **FAST** -WIDE SE / HVD: 20 MB/SEC (W) 1992 (PHYSICAL ONLY)
  - FAST 20 **(ULTRA)** SE/HVD: 40 MB/SEC (W) 1995 (PHYSICAL ONLY)
  - MANY OTHER DOCUMENTS FOR COMMANDS ETC (SPECIFIC KINDS OF PROTOCOL ONLY)

SCSI-X STOPS AFTER SCSI 3 - NEW PARADIGM STARTED BASED ON SPI-X (LOW LEVEL TRANSPORT LAYER) AND UPPER LAYERS (NOT LISTED HERE)

FOLLOWING ARE THE SPI-X VERSIONS UNDER THIS PARADIGM -- UPPER LAYERS CAN BE RUN ON THESE

- SPI-2 **(ULTRA 2)** LVD/HVD**: 80 MB/SEC (W) 1997 (PHYSICAL + LOWER LEVEL PROTOCOL)
- SPI-3 **(**ULTRA 3/**ULTRA 160**): 160 MB/SEC (W) 1999 (PHYSICAL + LOWER LEVEL PROTOCOL)
- SPI-4 (ULTRA 4/**ULTRA 320**): 320 MB/SEC (W) 2001 (PHYSICAL + LOWER LEVEL PROTOCOL)
- SPI-5 (ULTRA 5/**ULTRA 640**): 640 MB/SEC (W) 2003 (PHYSICAL + LOWER LEVEL PROTOCOL)

*MANY IMPORTANT PROTOCOL ENHANCEMENTS ADDED IN SCSI-2:E.G. SYNCHRONOUS DATA PHASE, MULTIPLE SPEEDS, MULTIPLE WIDTHS ETC -- FAST MODE SPECIFIED FOR USE WITH HVD (BUT NOT CLEARLY DOCUMENTED)

- ** ALL SPI-2 AND HIGHER USE LVD WITH OPTIONAL USE OF **ULTRA** SE MODE AT FAST 20 RATES, HVD DROPPED IN SPI-3 AND HIGHER

February 09, 2000

BILL HAM
COMPAQ COMPUTER CORP

SIGNAL INTEGRITY STRATEGIES

- SCSI HAS CONTINUED TO MINE THE PROPERTIES OF SILICON TO ALLOW EFFECTIVE USE OF ITS POTENTIALLY PROBLEMATIC MULTIDROP PHYSICAL ARCHITECTURE
- THESE PROPERTIES INCLUDE ALL OF THE FOLLOWING AT VARIOUS TIMES:
  - MORE PRECISE TIMING CONTROLS AND SIGNAL SPECIFICATIONS
  - USE OF ACTIVE NEGATION
  - USE OF DIFFERENTIAL SIGNALING
  - SIGNAL TRANSITION TIME CONTROL
  - SIMPLE RECEIVER FILTERING
  - ASYMMETRICAL DRIVERS
  - MULTIMODE DRIVERS
  - INCREASED USE OF LOGIC FOR COMPENSATION AND ADJUSTMENT (GATES ARE ALMOST FREE)
  - INTEGRATION OF ANALOG FUNCTIONALITY WITH DIGITAL CONTROL IN BOTH TRANSMITTERS AND RECEIVERS (E.G. ADAPTIVE FILTERING)
- BY SYSTEMATICALLY APPLYING THESE SILICON BASED TECHNIQUES IT IS POSSIBLE TO CONTINUE TO USE NEARLY THE SAME COPPER CABLE PLANT AND CONFIGURATION RULES AT EVER INCREASING SPEEDS
- THE USE OF EXPANDER TECHNOLOGY PROVIDES EVEN MORE SILICON BASED SCSI CAPABILITY

BILL HAM
COMPAQ COMPUTER CORP

SIGNAL INTEGRITY STRATEGIES CONTINUED

- THE NEMESIS OF MULTIDROP ARCHITECTURES IS FAST RISE AND FALL TIMES OF THE SIGNALS
- SHORTER TIMES INTENSIFY THE MAGNITUDE OF NOISE AND ALSO DECREASE THE SIZE OF THE PHYSICAL FEATURES THAT DISTURB THE SIGNALS
- SINCE (A) ONE OF THE BIGGEST DISTURBANCES COMES FROM THE STUBS ON THE SCSI DEVICES AND (B) THE SIZE OF DEVICES IS NOT CHANGING SIGNIFICANTLY AS THEY GET FASTER, MANAGEMENT OF RISE TIME EFFECTS IS VITAL
- PRESSURE FOR FASTER RISE TIMES COMES FROM LESS TIME REQUIRED FOR SIGNALS TO PASS THRU THE INDETERMINATE INPUT REGION FOR RECEIVERS AND FROM FASTER DATA RATES WITH LESS TIME BETWEEN BITS
- BY USING SILICON BASED COMPENSATION METHODS SUCH AS SKEW SUBTRACTION, JITTER CANCELING, ADAPTIVE FILTERING, AND MORE SENSITIVE RECEIVERS THAT HAVE SMALLER INDETERMINATE REGIONS ONE MAY RELIEVE THE PRESSURE ON DECREASED RISE TIMES
- PRESENTLY IT IS POSSIBLE TO KEEP THE SAME CONFIGURATION RULES THRU ULTRA 320 DUE TO NOT HAVING TO DECREASE THE RISE TIME BELOW THAT USED WITH ULTRA 2!!