SCSI signal modeling study group (SSM) 00-146r0
Huntington Beach, CA
Subject: Draft minutes for the SSM working group on February 08, 2000

This was the next meeting to address the general subject of modeling for parallel SCSI. Dean Wallace of Qlogic led the meeting. Bill Ham of Compaq took these minutes. There was a good attendance from a broad spectrum of the industry. QLogic(Skip Jones) hosted the meeting.

Last approved minutes: 00-111r1.

1. AGENDA SSM MEETING (ROCHESTER MN)

2. Introductions

Dean Wallace opened the meeting and conducted the introductions and reviewed the meeting purpose. He thanked Skip Jones of Qlogic for hosting the meeting.

3. Attendance

The following folks were present:

4. Attendance

The following folks were present:

Name	Company	E-Mail
Paul Aloisi	TI	Paul_Aloisi@TI.com
Larry Barnes	LSI	larry.barnes@lsil.com
Dave Chapman	Amphenol	dave.chapman@aipc.fabrik.com
Zane Daggett	Hitachi	zdaggett@hcm.hitachi.com
Rob Elliott	Compaq	Robert.Elliott@compaq.com
Jie Fan	Madison Cable	jfan@madisoncable.com
Don Getty	TI	Donald_Getty@TI.com
Bill Gintz	Seus	wcgintz@ix.netcom.com
Bill Ham	Compaq	bill_ham@ix.netcom.com
Thom Kreusel	HP	Thom_Kreusel@hp.com
Jay Neer	Molex	jneer@molex.com
Martin Ogbuokiri	Molex	mogbuokiri@molex.com
Doug Wagner	FCI	dwagner@fciconnect.com
Dean Wallace	Q-Logic	d_wallace@qlc.com
Mason Wong	Amp	mason.wong@amp.com

5. Agenda development

The agenda shown was that used.

6. Call for vice chair

Due to Jonathan Fasig not being available to continue his vice chair role Paul Aloisi agreed to accept the appointment to vice chair effective immediately.

7. Approval of previous minutes

The minutes of the last meeting were reviewed and minor changes were made. Bill Ham moved and Paul Aloisi seconded that these revised minutes be approved. Motion passed unanimously. This document will be posted as document 00-111r1.

8. Action item review

The action items were reviewed with the status indicated in the action item section of the minutes.

9. Presentation Policy

This item is included for easy reference and will be retained in future minutes.

It is the policy of the SSM working group that all material presented at the SSM working group shall be made available electronically and posted on the T10 web site.

Material presented at the meeting should be uploaded to the T10 web site two weeks prior to the meeting. Alternatively the material may be electronically supplied to the chair or secretary at the meeting where the material is presented at the discretion of the chair.

Material should be free from any statement of confidentiality or restriction of use and should not contain any pricing or product scheduling information.

10. SSM project proposal - Ham

The SSM project was approved at the November T10 plenary. The project number is 1414DT.

11. Presentations

11.1 Cable media model parameters - Jie Fan

Jie presented the methodology used in Madison for creating HSPICE models from RLGC parameters. This consists of an RLGC input into a test transfer tool box where conversion to an HSPICE occurs. This presentation was background information. It is expected that this parameter extraction process will be documented in SSM as an example.

11.2 IBIS status - Larry Barnes

Larry noted that the multilevel signal capability has now been incorporated into version 3.2? of IBIS. This does not incorporate the intelligence needed to execute a transmitter ISI compensation scheme where the output depends on the data pattern being transmitted. On the other hand if one uses a preprocessor to deliver the ISI compensation into the IBIS simulation environment then is seems possible to model an ISI precompensation scheme.

11.3 Positioning of SSM in the industry - Ham

Bill went over the activities presently underway in the industry (at least those that are publicly accessible) that relate to interconnect testing and modeling. These activities include the two going on in T10 (SPIP and SSM), 2 going on for serial copper and optical in SFF, and some modeling activity possibly in its infancy in T11.

It is very clear that amongst all these activities that the SSM activity is the only one that is addressing the entire system including the interoperability and is key to many activities. It is important that this activity continue until a complete document is created and viable models for all the components are available thru the web site.

A presentation containing this view needs to be created and delivered to the industry. Further, the availability of models for all the SCSI components will establish SCSI as the truly interoperable technology because users will be able to design systems with enough detail available during the design cycle.

11.4 Network parameters annex - Barnes

After some discussion it was decided that Larry will add this annex. This annex will describe the following: Networks, N-port networks, and conversion between two-port network parameters.

12. Matrix development for SSM

The following summarizes the present position for the SSM matrix. This matrix is a concise description of the methodology to be used for the respective areas of the point to point SCSI bus segment. Several of the areas were significantly modified at this meeting. Note that the multidrop areas have not yet been identified.

This section contains some repeated information from the last minutes as it continues to be relevant and current.

12.1 Transceiver chips: owner, Dean Wallace

No new content info this meeting.

Interface is at packaging pins
Model types: Spice, IBIS, HDL, table spice – details TBD
Data patterns: TBD
ISI compensation: required but not presently believed compatible with IBIS capability – this means that IBIS will have to be enhanced and that only SPICE models will be effective until the new IBIS techniques are available.
Single line required - cross talk from non SCSI sources not considered in the model, SCSI line cross talk is not significant within the

transceiver. Therefore multiline models are not required for transceivers.

Action Item: Dean to email folks who have open action items relating to transceivers.

12.2 Bus segment termination: owner, Paul Aloisi / Don Getty

No new content information.

Interface is at package pins
Model types: Spice, IBIS details TBD
Terminator type: multimode
Single line only

12.3 Transceiver board: owners, Tariq Abou-Jeyab and Matt Schumacher

No new content information.

Interface is at transceiver board connectors, transceiver chip pins, terminator chip pins
Model types: Spice
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

The present paradigm for this component follows:

Listed are some key datapoints to consider for HSPICE simulation of a simple LVD SCSI PCB. Initial simulations will be used to optimize PCB routing topologies. Simulating worst case scenarios will be discussed in a later document, as it will require SPICE model correlation, process corners, multiline SPICE models for cross talk etc.

Request SPICE models:

check for a driver and a receiver model
Ask for single line models and multiline models of connectors. Multiline models may take much longer to arrive if you can get them at all. If single line models are used, signal integrity investigation will not include crosstalk.
Are models for unmated connectors necessary?
Required models must work for various edge rates (slow, typ, fast)
Keep the models in a centralized/secure location. Vendors usually distribute them under NDA.
Some correlation of the models is recommended (compare simulation and lab data)
Request models well in advance of need

Obtain transmission line geometries from PCB data / design requirements

These parameters are required: trace width, copper weight of trace and planes, dielectric constants, dielectric spacing within the

differential pair, dielectric spacing to the planes and trace lengths of the nets to be simulated.

Generate RLGC matrices for transmission line segments(cline):

Using a field solver, obtain the RLGC matrices for the transmission line geometries.
Compare the field solver impedance with the TDR measurement of the coupon.
Note: the coupon will provide a controlled environment with minimal discontinuities for accurate trace characterization.

Draft a trace topology from the known trace segments and components:

Draft the transmission line topology
the drawing below is an example of a simple transceiver board in host bus adapter

Build a spice netlist for the trace topology:

Do not forget the process variations.

Simulate and review data:

Time domain simulation is sufficient for optimizing topologies.

W's are SPICE element numbers. All other numbers are node locations.

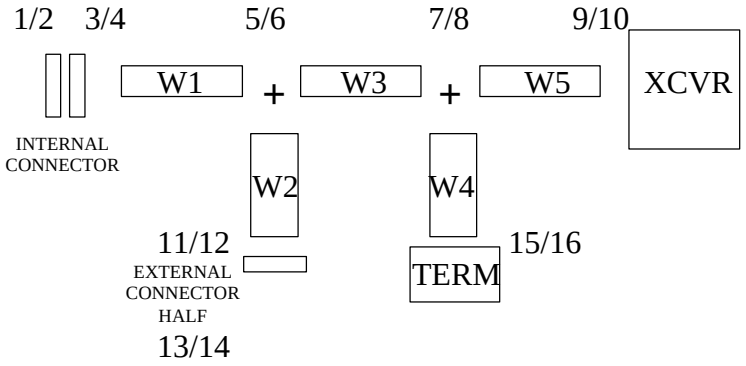


Figure 1 - Architecture of a transceiver board model (no unused connectors)

12.4 Mated connectors: owner, Martin Ogbuokiri

No new content information.

Interface is at transceiver board and the cable assembly transition region
Model types: Spice
Connector types: VHDCI, SCA-2, HD68
Mounting style: thru hole, SMT,

single line, multiline

Connector models are in place at the Molex web site and pointers are now in place on the T10 site.

12.5 Cable assembly transition region: owners, Bob Gannon, Greg Vaupotic

Interfaces are at the connector termination and the uniform media
Model types: Spice same as connector
Construction types: twisted flat, round fanout, laminated round, IDC flat?
Single line multiline

Although there was no new specific content for this matrix element it was noted that the parameter extraction methods described by Dima in his presentation may be excellent for extracting RGC for the cable transition region.

Action item: Rollie O'Groske to provide a plan to get a model for the transition regions.

12.6 Uniform cable media: owner, Jie Fan

Interfaces are at the beginning of the cable assembly transition region on either end.
Model types: Spice
Cable types: flat, round shielded, round unshielded twisted flat?
Single line, multiline

Action item: Jie to provide a cable media model to the web site.

12.7 Backplane: owner, Larry Barnes

Interfaces: connectors mounted on the backplane, directly mounted components,
Model types: SPICE
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

Issue: how to handle the unmated connectors on the backplane. Two sub issues: (1)lack of existence of unmated connector models and (2) convergence of the simulation with dangling open circuits. The latter can be handled by adding a high value resistance to the open circuit to "fool" the simulator.

Action item: Larry Barnes to supply component definition and a graphical representation for the backplane (should not contradict the transceiver board if possible)

13. Simulation integration strategy

Further discussion pending progress on the component level simulation work. This will be addressed at the next meeting.

14. System configurations

Not discussed but reaffirmed as needed for the document

15. Data patterns

A preliminary discussion of the issues involving data patterns was held. The following resulted:

Data patterns need to consider the following properties:

- Intersymbol interference effects on single lines
- Cross talk from other SCSI lines
- driver release effects (driven to hi Z)
- Residual jitter (clock like patterns)
- Word patterns as well as individual patterns
- SSO
- Worst case digital patterns
- Sinusoidal patterns

A spirited discussion concerning how to deal with receivers that modify the input signal (either adaptively or not) was held. Is this part of the signal path or not?

A more general concept of data pattern is possible with simulation because the inputs can be selected in the model. For example, skew from line to line and skew within the same line can be introduced. This latter was not considered in any detail but promises to be a significant benefit of modeling.

16. Data rate

Data transfer rates in SCSI are determined by more than the highest frequency content of the signals. Specifically, single transition, double transition, width, specific protocol variant and adaptive filtering affect the data rate. Therefore one must be careful in simulation to ensure that the relationship between the analog signals and the application is understood.

The following table will be added to the document that shows some of the relationships:

SCSI variant	REQ/ACK maximum frequency (MHz)	Data line maximum frequency (MHz)	Minimum rise / fall time (ns) (20-80%)	Maximum launch amplitude
SCSI-1 SE	async - NA	NA	NA	5.25V
SCSI-2 SE	5 MHz	2.5 MHz	NA	5.25V
SPI-1 SE	10 MHz	5 MHz	5 ns	5.25v
Ultra SE	20 MHz	10 MHz	5 ns	3.7v
Ultra2 LVD	40 MHz	20 MHz	1 ns	2.2 V DFpp
Ultra 160 LVD	40 MHz	40 MHz	1 ns	2.2 V DFpp
Ultra 320 LVD	80 MHz	80 MHz	1 ns	2.2 V DFpp
Ultra 640 LVD	160 MHz	160 MHz	???	???

17. Definitions:

A comprehensive set of definitions has been created in the draft document. Definitions from IEEE standard dictionary are used if available.

SPICE, IBIS, model, validation, cable assembly, transition region, verification, accuracy, HDL, VHDL, ASM, ASCM, Veriloq, PCB, backplane, microstrip, stripline, via, discontinuity, cline, lossy, lossless, uniform, attenuation, gain, differential, planar, skin effect, dielectric constant, dielectric loss, loss tangent, conductivity, resistivity, convergence, phase velocity, group velocity, group delay, phase delay, multiline, single line, SLM, MLM, single ended, balanced, unbalanced, mode, element, RLGC, netlist, admittance, transmittance, coupling(K), matrix, S parameters, scattering matrix, ABCD, Y parameters, two-port parameters, and others to be suggested later.

18. Model database strategy (Wallace)

The revised proposed a specific summary of the present plans for the web based database:

- List of companies with existing models.
- What type of models are they. Connector media, transceiver etc.
- Description / intended use
- Path to the model, is an nda required for the model
- Contact info for model support
- What type of model, SPICE, IBIS, HDL.
- Revision history on site.

19. Tools:

This item refers to software tools that may be useful for SSM.

Note that IBIS is not a tool but rather is a behavioral specification for I/O buffers and other stuff such as terminators and connectors. IBIS is described separately.

Following is a list of the major tools and the basic relationship between them:

Simulation tools:

- SPICE-like
  - HSPICE
  - Berkeley SPICE
  - Contec SPICE
  - PSPICE
- Behavioral
  - HDL
  - VHDL
  - Verilog
  - Hyperlynx
  - Viewlogic XTK
- High frequency structural simulator
  - Ansoft
  - HP-ADS (advanced design simulator)

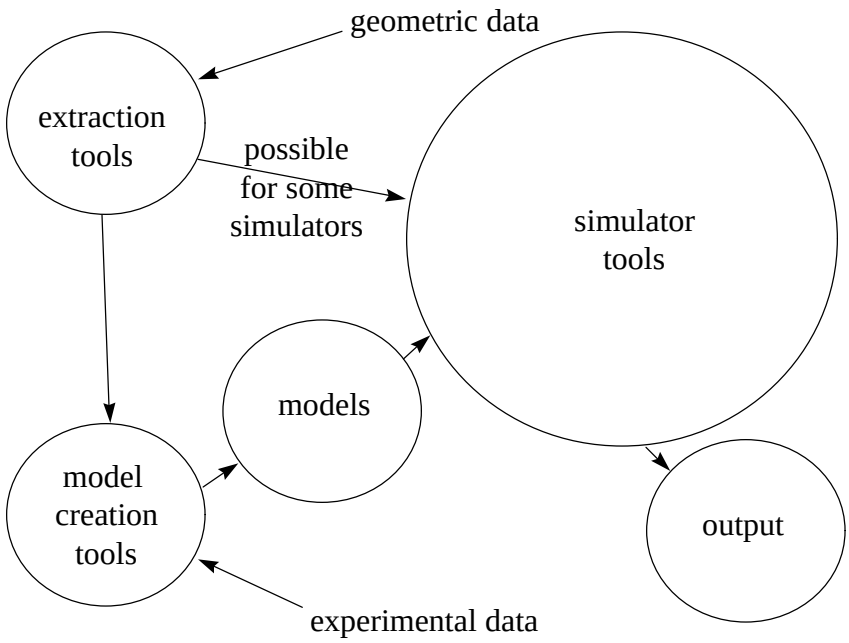
Extraction tools

- Maxwell
  - Maxwell-2D
  - Maxwell-3D
- Pacific Numerix

Model creation tools

- Mentor Graphics
- Cadence
- HP suite

The following figure shows the relationship between the different tool classes:



20. Document framework (Barnes)

Larry Barnes, editor of the SSM document, reviewed the present state and organization of the document. Following is the result of this discussion cast in the form of a table of contents with owners assigned. The numbering may not be accurate in the list below. Note the addition of Dima to the cable assemblies section.

Section owners are to create basic material and submit to Larry Barnes before the next meeting.

1. SCOPE ((Larry Barnes)
2. REFERENCES(Jonathan Fasig)
2.1 Approved references
2.1.1 References under development
2.2 Resources
2.2.1 Publications
2.2.2 Online bookstores & publishers
2.2.3 Other online resources
2.3 Tools
3. DEFINITIONS, ACRONYMS, SYMBOLS, KEYWORDS, AND CONVENTIONS (group)
3.1 Definitions
3.2 Acronyms
3.3 Symbols and Abbreviations
3.4 Keywords
3.5 Conventions
4. GENERAL
4.1 Overview (Bill Ham)
5. METHODOLOGIES
6. MODELS
6.1 General recommendations (Larry Barnes)

6.1.1 Supporting documentation
6.1.2 Behavioral models
6.1.3 Circuit Models
6.2 Cables
6.2.1 Cable media (bulk cable) (Jie Fan)
6.2.2 Transition region (Bob Gannon, Greg Vaupotic)
6.3 Connectors (Martin O.)
6.3.1 Cable connectors
6.3.2 Non-cable connectors
6.3.2.1 RLC transmission line matrix
6.4 Printed circuit boards (Matt S., Tariq A.)
6.4.1 Traces
6.4.1.1 Microstrip
6.4.1.2 Stripline
6.4.1.3 Broad coupled stripline
6.4.1.4 Offset broad coupled stripline
6.4.2 Discontinuities
6.4.2.1 Vias
6.4.2.2 Pads
6.5 Devices
6.5.1 Terminators (Paul Aloisi / Don Getty)
6.5.2 Transceivers (Dean Wallace)
6.5.3 Packages
7. STANDARD MODEL CONSTRUCTIONS
7.1 Host bus adapter / target board (Tariq / Matt S.)
7.2 Point to point / multidrop (TBD)
7.3 Cable assemblies (Dima Smolyansky)
7.4 Backplane (Larry Barnes)
7.5 System model (TBD)
8. MEASUREMENT AND VALIDATION
8.1 Access to measurement points
8.2 Physical measurement points (Greg Vaupotic)
8.3 Behavioral
8.4 Circuit
9. SIMULATION INTEGRATION STRATEGY (Dean Wallace)
9.1 System configurations
9.2 Data patterns
9.3 Data rates

21. New business

No new business was conducted.

22. Next meetings

Scheduled meetings:
Mar 01, 2000 Manchester,NH (Hitachi) 9AM to 5PM
April 12, 2000 Monterey, CA (Adaptec) 9AM to 5PM

It was proposed that SSM go to a one working group meeting between T10 plenaries after the April meeting (i.e. skip May do June skip July do August etc). Extending the meeting to a 1.5 day format every two months seemed to meet with agreement. This does not preclude synchronizing with SPI-4 schedules but does not guarantee it either.

Next meeting for SSM proposed for June 13 1:30PM to June 14. (SPIP will be June 12 9 AM to June 13 12 noon.) Tentative location is Lisle, IL hosted by Molex.

23. Action Items:

23.1 Action items from previous meetings

Status as of the February 08, 2000 meeting is shown.

Larry Barnes to do an overview presentation of the IBIS transceiver model specification.
Status: done

Ham to post the draft minutes of the Dec 01 meeting after review by Dean
Status: done

Larry Barnes to propose a multilevel output capability for IBIS to allow for ISI compensation.
Status: done for multilevel, ongoing for ISI compensation

All matrix element (document section) owners to provide draft input for the respective sections to Larry Barnes by November 19, 1999. (Provide input in Word 6/7 format) send to larry.barnes@lsil.com
Status: input received from Jonathan F and Don Getty – others have not yet responded - action item carried over to next meeting.

Larry Barnes to contact John Lohmeyer to expedite the creation of the SCSI modeling web site.
Status: done

Action item: Dan Smith to provide Seagate transceiver models to the web site.
Status: carried over

Action item: Tariq to provide Adaptec transceiver models to the web site.
Status: carried over

Action item: Larry Barnes to provide LSI transceiver models to the web site.
Status: carried over

Action item: Paul A. to provide web site info for the TI terminator models.
Status: carried over

Action item: Rollie O’Groske to provide a plan to get a model for the transition regions.
Status: carried over

23.2 New action items from present meeting

Dean to send emails to all folks with open action items on Tuesday of each week (until the action item is completed).
Status: new

Ham to post the draft minutes of the February 08 meeting after review by Dean and the approved minutes of the December meeting.
Status: new

Larry Barnes to supply component definition and a graphical representation for the backplane (should not contradict the transceiver board if possible)
Status: new

24. Adjourn

The meeting adjourned at 6:00 PM