Quantum™

T10/00-133r3

Ultra320 SCSI Calibration and Clock Protocol

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Edits from Rev2

- In rev2, a 50ns pause was inserted between the high frequency (101010…) pattern, and the low frequency (11001100…) pattern.
- In this rev, the pause has two distinct sections:
  - In the initial 50ns, the free-running clock continues to run
  - This is followed by a second 50ns pause, in which the clock is also paused
- The 11001100 pattern has been extended to 24 clocks (300ns) minimum
- Pattern duration is now specified in clock ticks instead of time.
- Removed references to calibration following PPR; calibration now done on every connection

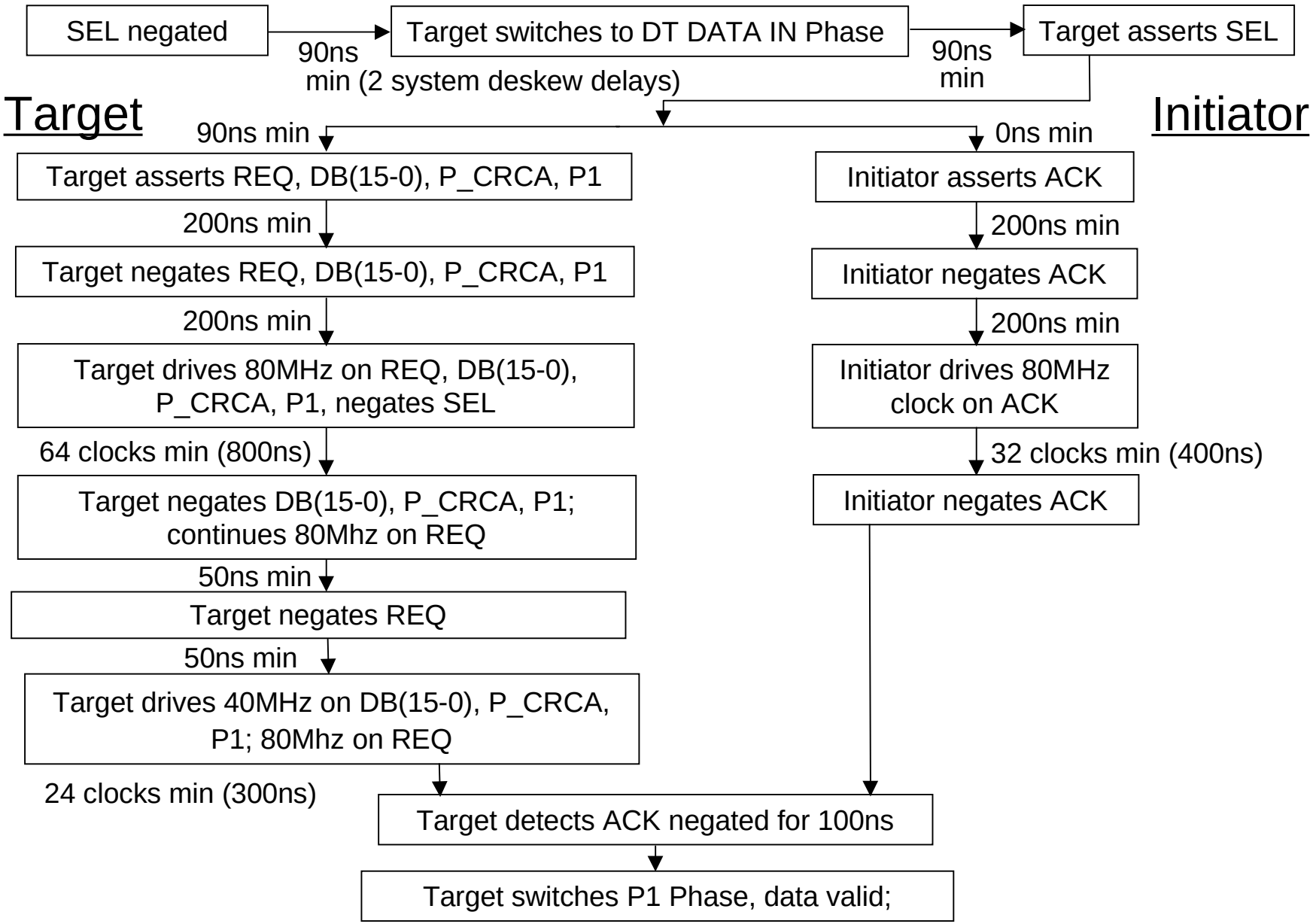
Training Protocol

- The initiator selects when training will occur using a new field in the PARALLEL PROTOCOL REQUEST message.
- Training may occur:
  1) Before the first DT DATA IN and DT DATA OUT phase for every nexus if information unit transfers are enabled, or
  2) As a complete training sequence (DATA IN and DATA OUT) immediately after a PPR message.
- The target initiates a training pattern by switching to a DT DATA phase and then asserting SEL.

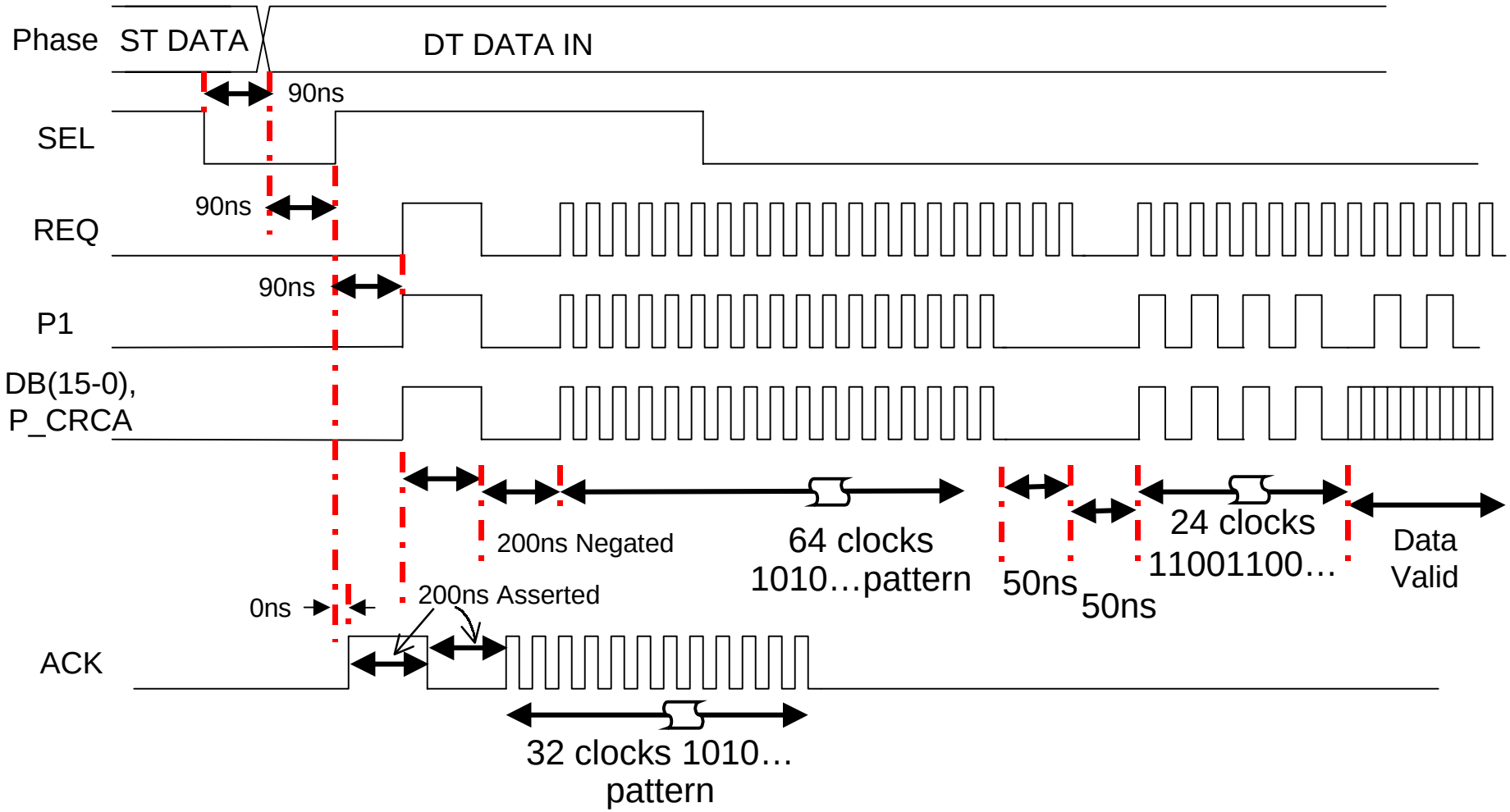
DATA IN Training

- The target transmits training patterns on REQ, DB(15-0), P_CRCA (a.k.a. P0), and P1.
- The initiator performs adaptive equalization on REQ, then applies the result to REQ, DB(15-0), P0, and P1
- The initiator performs skew compensation on DB(15-0), P0, and P1.
- The initiator transmits training patterns on ACK.
- The target performs adaptive equalization on ACK.
- If this sequence is to be followed by data, the target begins transferring data at the end of the sequence.
- If this sequence is to be followed by a DATA OUT training sequence, the target negates REQ, releases DB(15-0), P0, and P1 and switches to DT DATA OUT.

DATA IN Training Flow Diagram



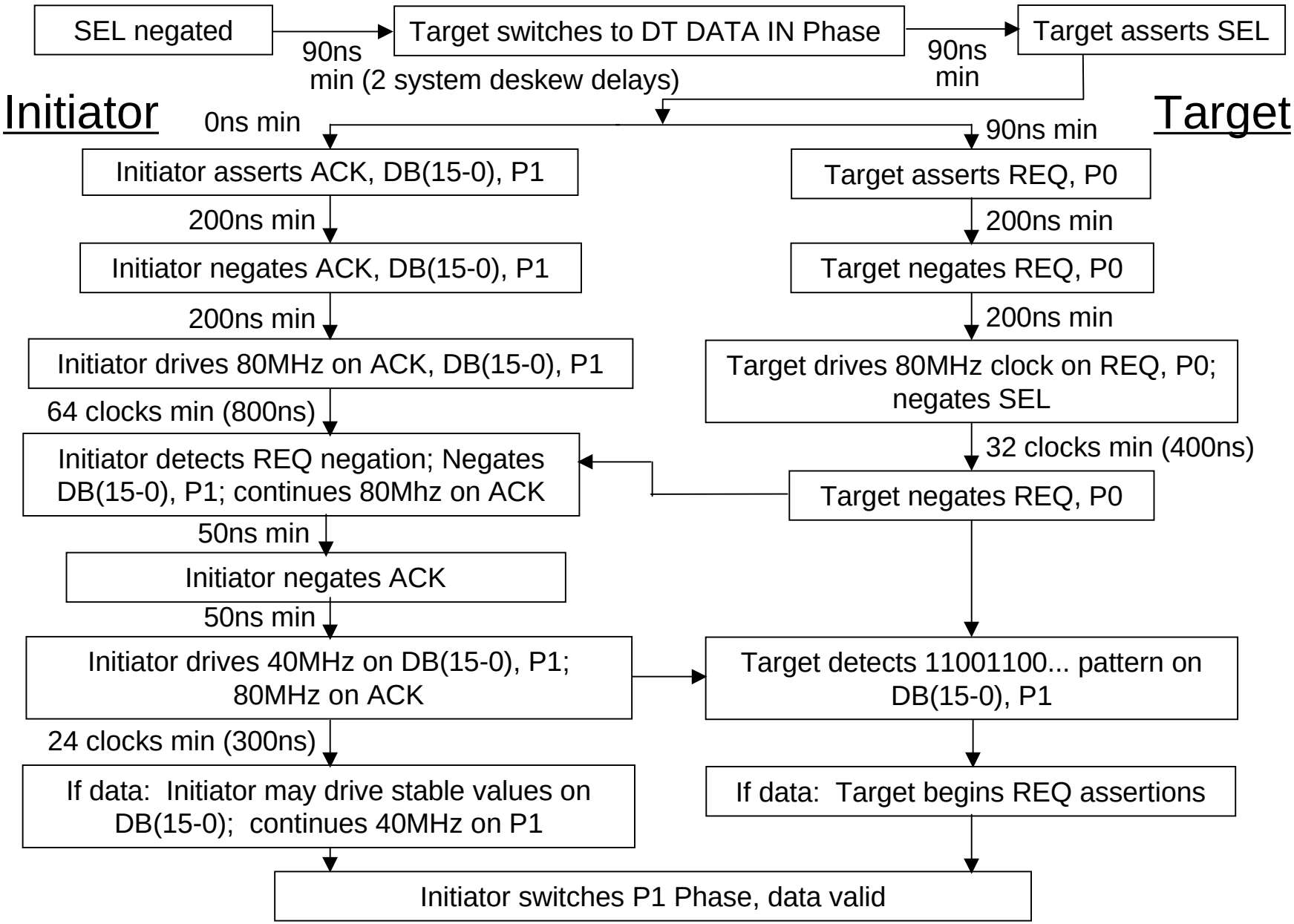
DATA IN Training Timing



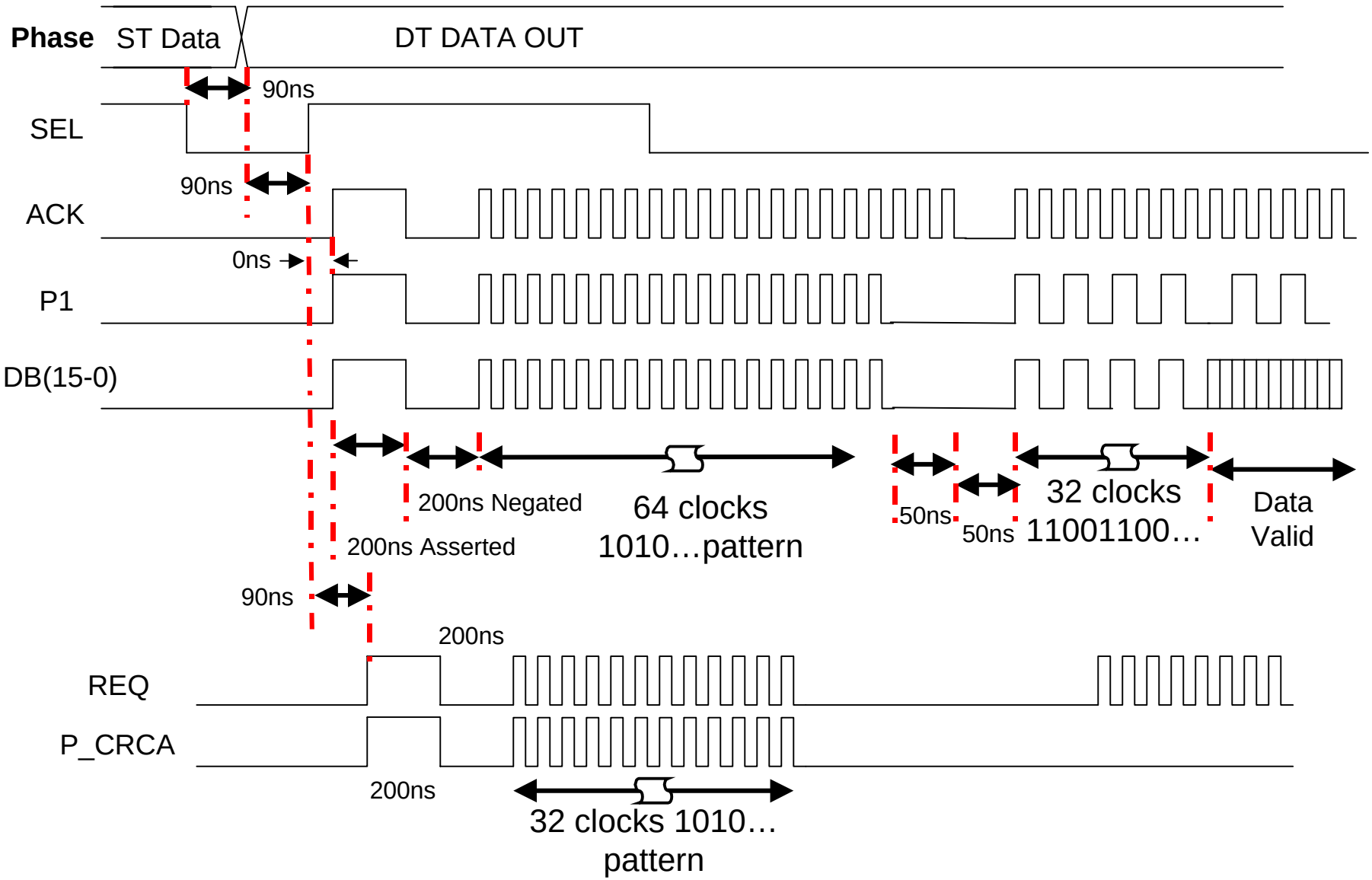
DATA OUT Training

- The initiator transmits training patterns on ACK, DB(15-0), and P1.
- The target performs adaptive equalization on ACK, then applies the result to ACK, DB(15-0), and P1
- The target performs skew compensation on DB(15-0) and P1.
- The target transmits training patterns on REQ and P0.
- The initiator performs adaptive equalization on REQ.
  - At 80Mhz, REQ will not reach full amplitude in some configurations.
    - Equalization is necessary for reliable edge detection.
    - The Adaptive Equalization result is applied to P0 to enhance noise margin.
  - Skew compensation is avoided on P0 by requiring extra setup and hold margin when P0 transitions -- which is a rare event.
- The target then begins transmitting REQs, the initiator begins transferring data at the end of the sequence.

DATA OUT Training Flow Diagram



DATA OUT Training Timing



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Starting Clock when not Training

- The target DOES NOT assert SEL at start of the DT DATA phase.
- For DT DATA IN:
  - The target begins the free running clock 400ns after the phase change (800ns if this is following a DT DATA OUT phase).
  - The target drives P1 with a constant phase (invalid data) for a minimum of 16 clocks to give the initiator time to establish phase of P1 signal.
  - The target can then begin the data transfer.
- For DT DATA OUT:
  - This is similar to the calibration protocol.
  - The initiator drives the clock on ACK and establishes the P1 phase after detecting the phase change.
  - This is proposed to be 90ns min (this allows for filtering on phase lines).
  - The target does not drive REQ until it detects the clock on ACK and establishes the phase of the P1 signal. The target must also wait the 400ns minimum phase change time.
  - The initiator cannot change P1 phase and send data until it receives REQs from the target.

Ending the Phase: DT DATA OUT

- The initiator is transmitting the free-running clock on ACK.
- After the transfer is complete the target changes phase (e.g., to BUS FREE).
- When the initiator detects a change in the phase lines it will negate ACK within 200ns.
- When the target changes phase, it will wait a minimum of 800ns before asserting REQ or monitoring ACK. ACK transitions within the 800ns time will be ignored.
- The 800ns number:
  - 200ns prop delay from target to initiator
  - 200ns for initiator to negate ACK
  - 200ns prop delay from initiator to target
- This is more than 400ns, so use 800ns, since those are the two existing choices during a phase change.

Ending the Phase: DT DATA IN

- The target is transmitting the free-running clock on REQ.
- The target stops transmitting the clock when it has transmitted all data and received all ACKs.
- Once the clock is stopped, the target cannot resume data transmission. The target must change phase (e.g., to BUS FREE).