Quantum™

T10/00-133r0

Ultra320 SCSI Calibration Protocol

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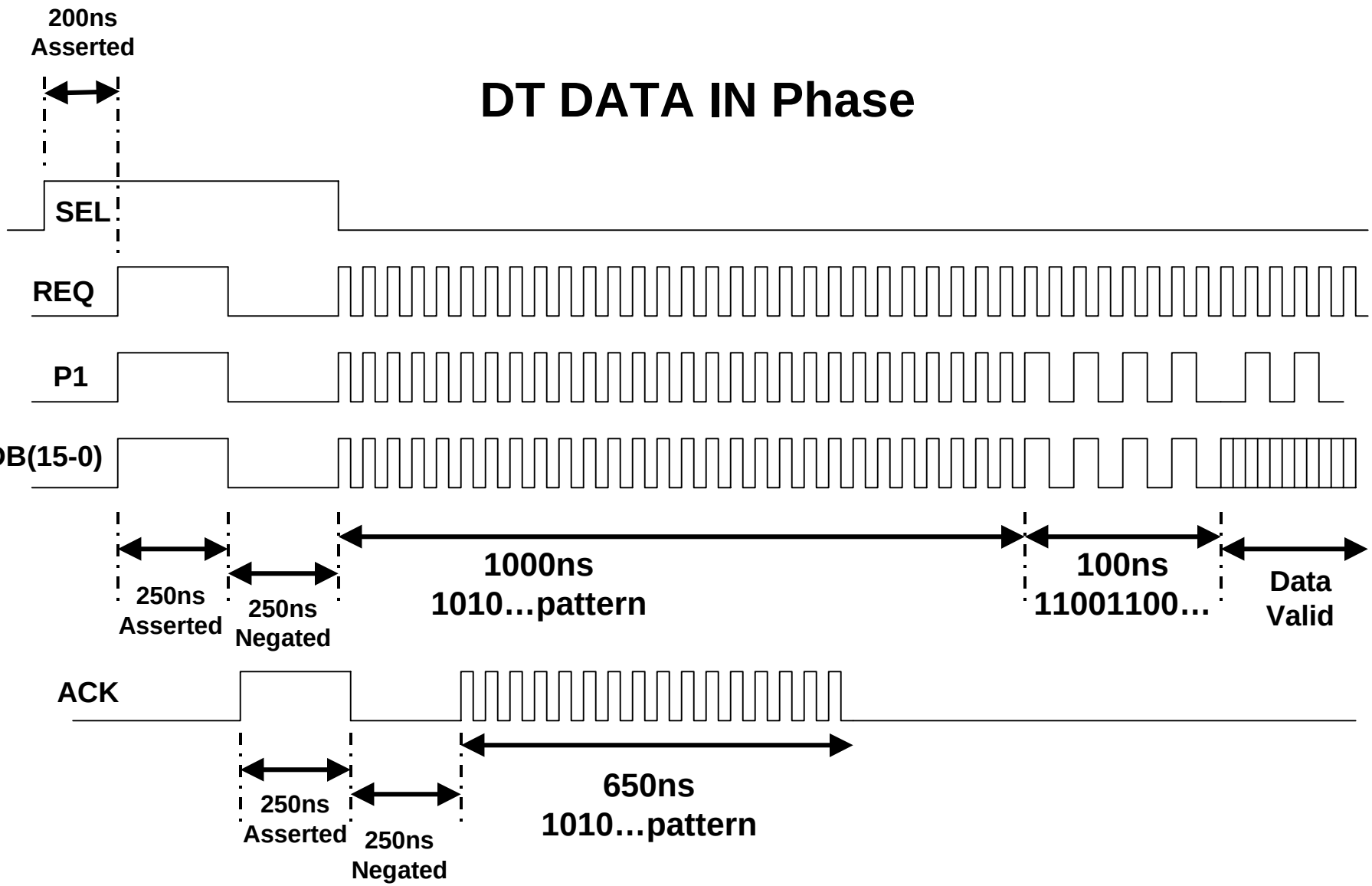
Calibration Time

- **Major calibration at the beginning of every DT DATA phase**
  - **Simplicity - no need to remember all parameters for each I_T pair from one connection to the next**
  - **Easier for expander chips**
- **Assumption:**
  - **Expanders (transceivers) must be able to easily detect the training pattern**
  - **Expanders cannot snoop the PPR message to determine an I_T pair are in U320 mode**
    - **Complex sequence to monitor**
    - **Errors during PPR negotiation aren't detectable by expander; error causes different result at negotiation completion than expander expects.**
- **Proposal - use assertion of SEL during DT DATA IN or DT DATA OUT to mark calibration cycle.**

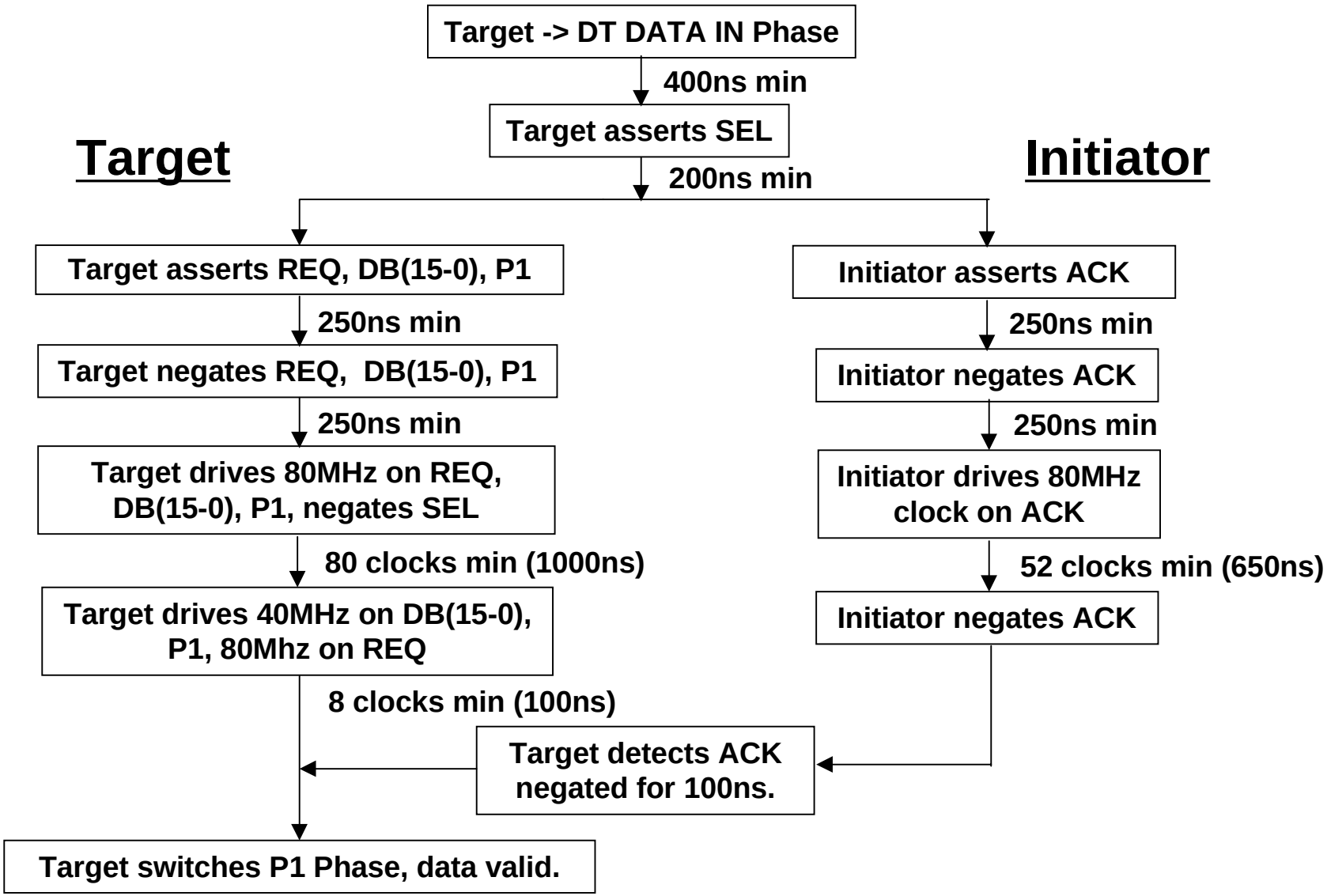
Signals to Calibrate

- **DT DATA OUT Phase**
  - **Adaptive equalization in target on ACK - then apply result to equalize ACK, DB(15-0), P1**
  - **Skew compensation in target on DB(15-0), P1**
  - **Adaptive equalization in initiator on REQ**
  - **At 80Mhz, REQ will not reach full amplitude in some configurations**
    - **Equalization necessary for reliable edge detection**
    - **Adaptive Equalization result applied to P0 enhances noise margin**
  - **Avoid skew compensation on P0 by requiring extra setup and hold margin when P0 transitions - a rare event.**
- **DT DATA IN Phase**
  - **Adaptive equalization in initiator on REQ - then apply result to REQ, DB(15-0), P0, and P1**
  - **Skew compensation in initiator on DB(15-0), P0, and P1**
  - **Adaptive equalization in target on ACK**
  - **Cannot have larger setup/hold on P0 - REQ is free-running clock**

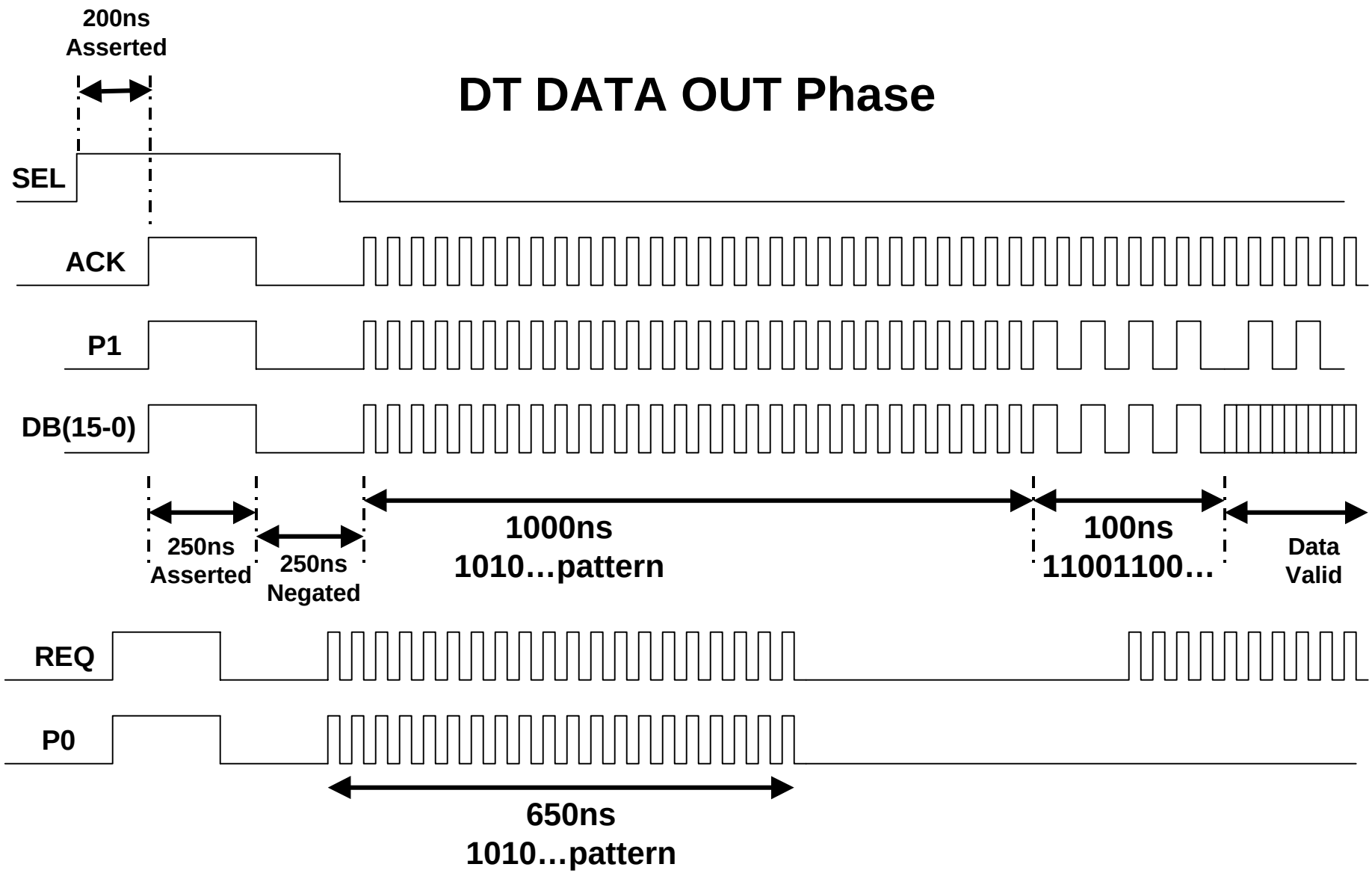
DT DATA IN Timing Diagram



DT DATA IN Calibration Flowchart



DT DATA OUT Timing Diagram



DT DATA OUT Cal Flowchart