Quantum™
Quantum Corporation
500 McCarthy Boulevard
Milpitas, CA 95035 USA

To: **T10 Technical committee**
From: **Mark Evans**
Bruce Leshay
Phone: 408-894-4019
Fax: 408-952-3620
Email: mark.evans@quantum.com
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Subject: Proposal for training pattern protocol to be included in SPI-4

Introduction

For parallel SCSI transfer rates of 320 and 620 megabytes per second, skew compensation and equalization will be performed at the receiver on data and clock signals and equalization will be performed at the transmitter on clock signals in order to achieve the required timings and signal quality. This scheme could also be used to provide improved signal quality at lower transfer rates. In order to perform these operations, a specified training pattern must be sent by both the transmitter and receiver on specified signal lines during a specified time in a specified manner. The following is a proposal that defines the elements required for a training pattern.

Revision 1 of this proposal has been updated to decrease the overall time required for each training pattern, to include flow diagrams of the training pattern sequences, and to provide a method for the application client to specify training, 1) before every DT DATA phase, 2) after a PPR message, or 3) before the first DATA IN and the first DATA OUT transfer of a nexus.

The clauses referenced in this proposal are relative to the draft standard SCSI Parallel Interface – 3 (SPI-3) revision 13a. That document is available at ftp://ftp.t10.org/t10/drafts/spi3/spi3r13a.pdf.

4.9.3.x DT DATA phase training patterns and receiver calibration

The training pattern sequences provides for defined patterns to be transferred on data, clock, and data qualifier signals so that the receiver of the signals may perform skew compensation, equalization or other calibration operations to improve signal quality. When to initiate a training pattern sequence is determined by the PARALLEL PROTOCOL REQUEST message. Depending on the content of the CAL_REQ field in the PARALLEL PROTOCOL REQUEST message, the training pattern sequences may be initiated by the target:

a) before every DT DATA phase, or
b) if information unit transfers are enabled, before the first DATA IN and the first DATA OUT transfer of a nexus, or
c) after a PARALLEL PROTOCOL REQUEST message is validated.

If an initiator selects that the training pattern sequences are to be performed after a PARALLEL PROTOCOL REQUEST message is validated, the initiator may then use this mechanism to request training pattern sequences after specific events (i.e., when the initiator detects that the topology of the bus has changed by the addition or removal of a device). If this mechanism is enabled and the target detects that training pattern sequences should be performed, the target may send a SYNCHRONOUS DATA TRANSFER REQUEST message to the initiator that could result in a new PARALLEL PROTOCOL REQUEST negotiation and training pattern sequences.

After a DT DATA IN training pattern sequence is initiated the target drives REQ, DB(15-0), P0, and P1 with the specified pattern. The initiator performs equalization on REQ, DB(15-0), P0, and P1. The initiator performs skew compensation on DB(15-0), P0, and P1. The initiator may also perform other operations on REQ, DB(15-0), P0, and P1 at this time. During this time the initiator drives ACK with the specified pattern. The target performs equalization and other operations on that signal.

After a DT DATA OUT training pattern sequence is initiated the initiator drives ACK, DB(15-0), and P1 with the specified pattern. The target performs equalization on ACK, DB(15-0), and P1. The target performs skew compensation on DB(15-0) and P1. The target may also perform other operations on REQ, DB(15-0), and P1 at this time. During this time the target drives REQ and P0 with the specified pattern. The initiator performs equalization and other operations on those signals.

A training pattern sequence following validation of a PARALLEL PROTOCOL REQUEST message consists of one DT DATA IN training pattern sequence followed by a DT DATA OUT training pattern sequence.

Skew compensation, equalization, and other operations performed by the receiver to improve signal quality are vendor specific and not defined in this standard. See 10.8.3.3 for definition of the specific training pattern sequence.

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9.1 SCSI parallel bus timing values

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Table 29 - SCSI bus control timing values

Subclause	Timing description	Type	Description
	.....		
9.2.35	System Deskew delay	minimum	45 ns
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9.2.a	Initial training time	minimum	200 ns
9.2.b	First transmitter training time	minimum	800 ns
9.2.c	Second transmitter training time	minimum	100 ns
9.2.d	Receiver training time	minimum	400 ns
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9.2.a Initial training time

This time is used by the transmitter and receiver during the first part of a training pattern sequence.

a) It is the minimum time that a target shall assert REQ, DB(15-0), P_CRCA, and P1 after asserting SEL at the beginning of a DT DATA IN training pattern sequence.

b) It is the minimum time that a target shall negate REQ, DB(15-0), P_CRCA, and P1 after asserting REQ, DB(15-0), P_CRCA, and P1 at the beginning of a DT DATA IN training pattern sequence.
c) It is the minimum time that an initiator shall assert ACK after detecting the assertion of SEL at the beginning of a DT DATA IN training pattern sequence.
d) It is the minimum time that an initiator shall assert ACK, DB(15-0), and P1 after detecting the assertion of SEL at the beginning of a DT DATA OUT training pattern sequence.
e) It is the minimum time that an initiator shall negate ACK, DB(15-0), and P1 after asserting ACK, DB(15-0), and P1 at the beginning of a DT DATA OUT training pattern sequence.
f) It is the minimum time that a target shall assert REQ and P1 after asserting SEL at the beginning of a DT DATA OUT training pattern sequence.
g) It is the minimum time that a target shall negate REQ and P1 after asserting REQ and P1 at the beginning of a DT DATA OUT training pattern sequence.

9.2.b First transmitter training time

This is the minimum time that a target or initiator transmits training pattern 1 (see 10.8.3.3).

9.2.c Second transmitter training time

This is the minimum time that a target or initiator transmits training pattern 2 (see 10.8.3.3).

9.2.d Receiver training time

This is the minimum time that a target or initiator transmits training pattern 3 (see 10.8.3.3).

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10.8.3.3.x DT DATA IN training pattern sequence

Following a selection or reselection, the target shall not transition to DT DATA IN phase for a training pattern sequence until at least two system deskew delays after it detects SEL negated. The target shall not initiate a training pattern sequence until at least two system deskew delays after transitioning to a DT DATA IN phase. The target shall initiate a training pattern sequence by asserting SEL. After asserting SEL, the target shall wait at least two system deskew delays and then assert REQ, DB(15-0), P0, and P1. The target shall wait at least initial training time and then negate REQ, DB(15-0), P0, and P1.

After negating REQ, DB(15-0), P0, and P1, the target shall wait at least one initial training time and then begin alternately asserting and negating REQ every (transfer period ÷ 2) ns (i.e., an alternating “101010...” pattern) and transmit the first transmitter training pattern by alternately asserting and negating DB(15-0), P0, and P1 every (transfer period ÷ 2) ns for at least one first transmitter training time. Assertion and negation of REQ, DB(15-0), P0, and P1 shall be in phase.

The target may negate SEL after beginning the alternate assertion and negation of REQ, DB(15-0), P0, and P1. The target shall negate SEL before beginning the second training pattern.

After transmitting the first transmitter training pattern for at least one first transmitter training time, the target shall transmit the second transmitter training pattern by alternately asserting and negating DB(15-0), P0, and P1 every (transfer period) ns (i.e., an alternating “110011001100...” pattern) for at least one second transmitter training time. Assertion and negation of REQ, DB(15-0), P0, and P1 shall be in phase. The target may test ACK.

After transmitting the second transmitter training pattern for at least one second transmitter training time, the target shall negate DB(15-0) and P0 for at least (transfer period × 2) ns. After negating DB(15-0) and P0 for at least (transfer period × 2) ns, the target shall test ACK.

If ACK is negated and this is a DT DATA IN training pattern before a DT DATA IN transfer, the target may begin transmitting data for the phase. If ACK is negated and this is a DT DATA IN training pattern after a PARALLEL PROTOCOL REQUEST message, the target shall negate REQ, release DB(15-0), P0, and P1, and switch to DT DATA OUT phase.

After detecting the assertion of SEL, the initiator shall assert ACK. After asserting ACK the initiator shall wait at least one initial training time and then negate ACK. After negating ACK the initiator shall wait at least one initial training time. The initiator shall then transmit a receiver training pattern by alternately asserting and negating ACK every (transfer period ÷ 2) ns (i.e., an alternating “101010...” pattern) for at least one receiver training time. After alternately asserting and negating ACK for at least one receiver training time, the initiator shall negate ACK.

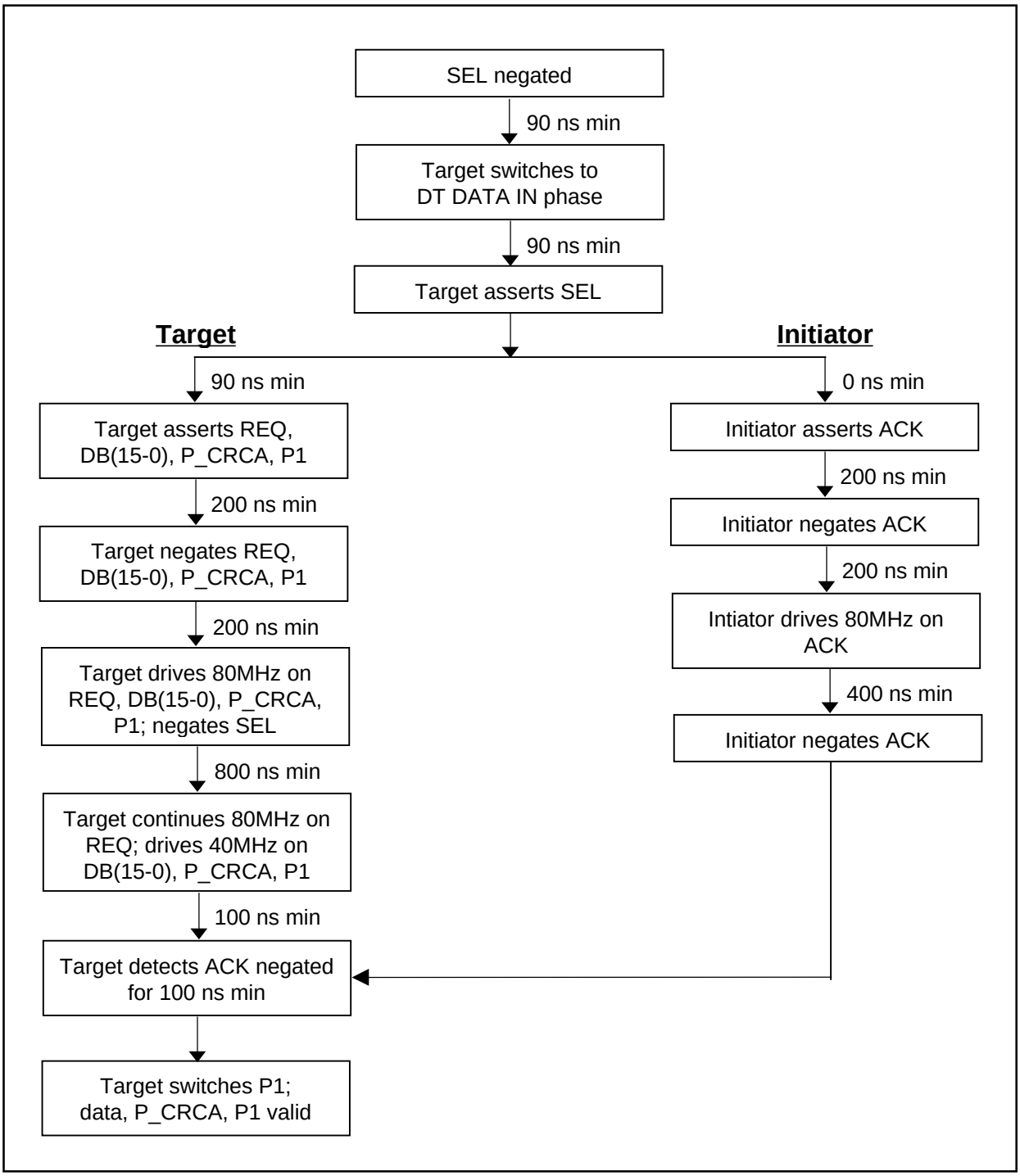

Figure x1 – Flow diagram for DT DATA IN training pattern before a DT DATA IN transfer

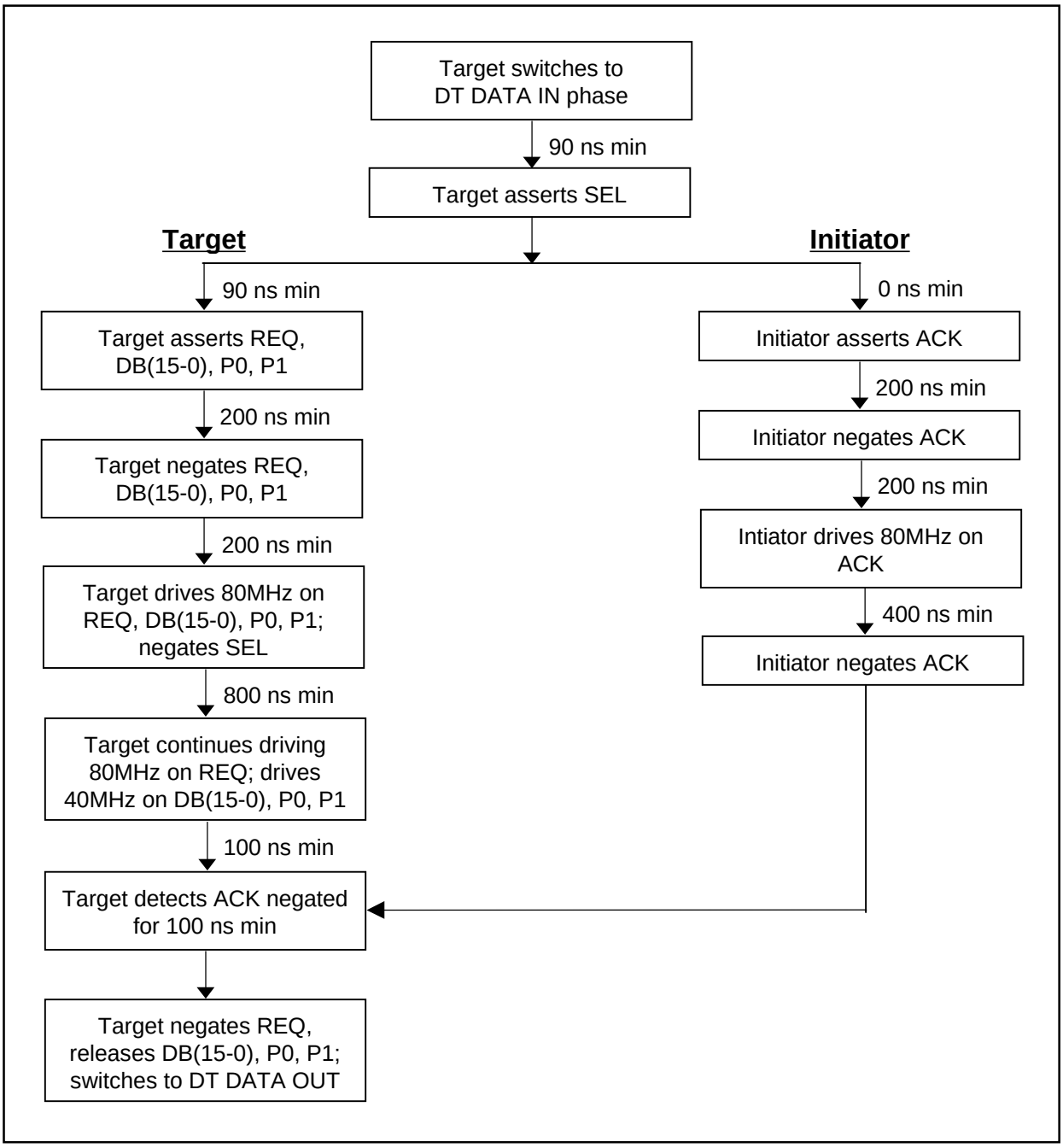

Figure x2 – Flow diagram for a DT DATA IN training pattern after a PARALLEL PROTOCOL REQUEST message

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10.8.3.3.y DT DATA OUT phase training pattern sequence

Following a selection or reselection, the target shall not transition to DT DATA OUT phase for a training pattern sequence until at least two system deskew delays after it detects SEL negated. The target shall not initiate a training pattern sequence until at least two system deskew delays after transitioning to a DT DATA OUT phase. The target shall initiate a training pattern sequence by asserting SEL. After asserting SEL, the target shall wait at least two system deskew delays and then assert REQ and P0. The target shall wait at least initial training time and then negate REQ and P0.

After negating REQ and P0, the target shall wait at least one initial training time and then transmit the receiver training pattern by alternately asserting and negating REQ and P0 every (transfer period ÷ 2) ns for at least one receiver training time. After alternately asserting and negating REQ and P0 for at least one receiver training time, the target shall negate REQ and P0. The target may negate SEL one initial training time after beginning the alternate assertion and negation of REQ and P0.

After detecting the assertion of SEL, the initiator shall assert ACK, DB(15-0), and P1. After asserting ACK, DB(15-0), and P1, the initiator shall wait at least one initial training time and then negate ACK, DB(15-0), and P1.

After negating ACK, DB(15-0), and P1, the initiator shall wait at least one initial training time and then begin alternately asserting and negating ACK every (transfer period ÷ 2) ns and transmit the first transmitter training pattern by alternately asserting and negating DB(15-0) and P1 every (transfer period ÷ 2) ns for at least one first transmitter training time. Assertion and negation of ACK, DB(15-0), and P1 shall be in phase.

The initiator shall continue to transmit the first transmitter training pattern for at least one first transmitter time or until detecting the negation of REQ for at least one system deskew delay after the receiver training pattern, whichever occurs last. After transmitting the first training pattern, the initiator shall transmit the second transmitter training pattern by alternately asserting and negating DB(15-0) and P1 every (transfer period) ns for at least one second transmitter training time. Assertion and negation of ACK, DB(15-0), and P1 shall be in phase. After transmitting the second training pattern for at least one second transmitter training time, the initiator may negate DB(15-0).

If this is a DT DATA OUT training pattern before a DT DATA OUT transfer, the target may begin transmitting REQ pulses for the data phase after detecting the initiation of the second transmitter training pattern on P1. The initiator may begin transferring data for the phase as soon as the second transmitter training pattern is complete and REQ pulses are detected from the target.

If this is a DT DATA OUT training pattern after a PARALLEL PROTOCOL REQUEST message, the initiator shall negate ACK, release DB(15-0) and P1. Upon detecting the negation of ACK, the target shall transition to BUS FREE.

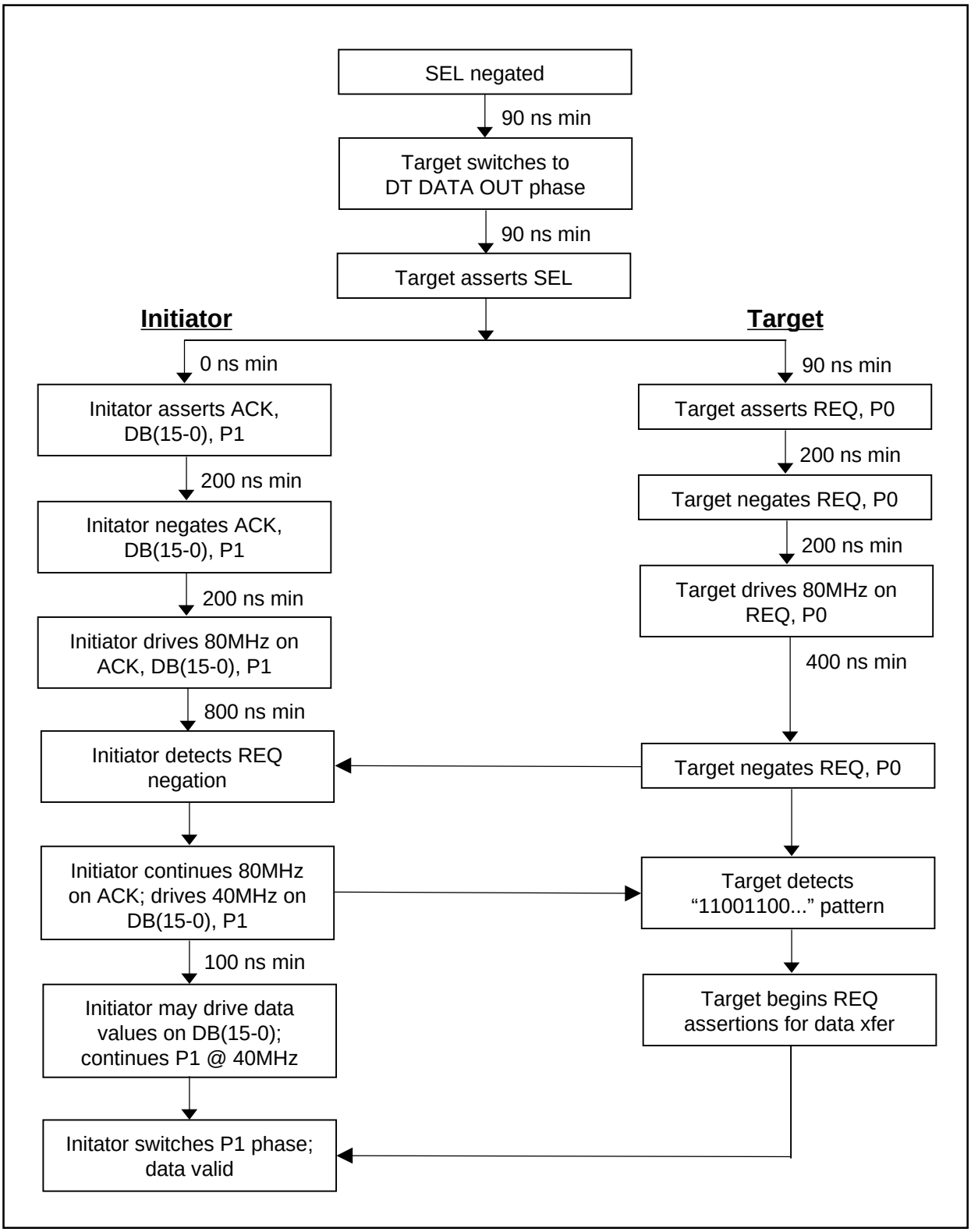

Figure x3 – Flow diagram for DT DATA OUT training pattern before a DT DATA OUT transfer

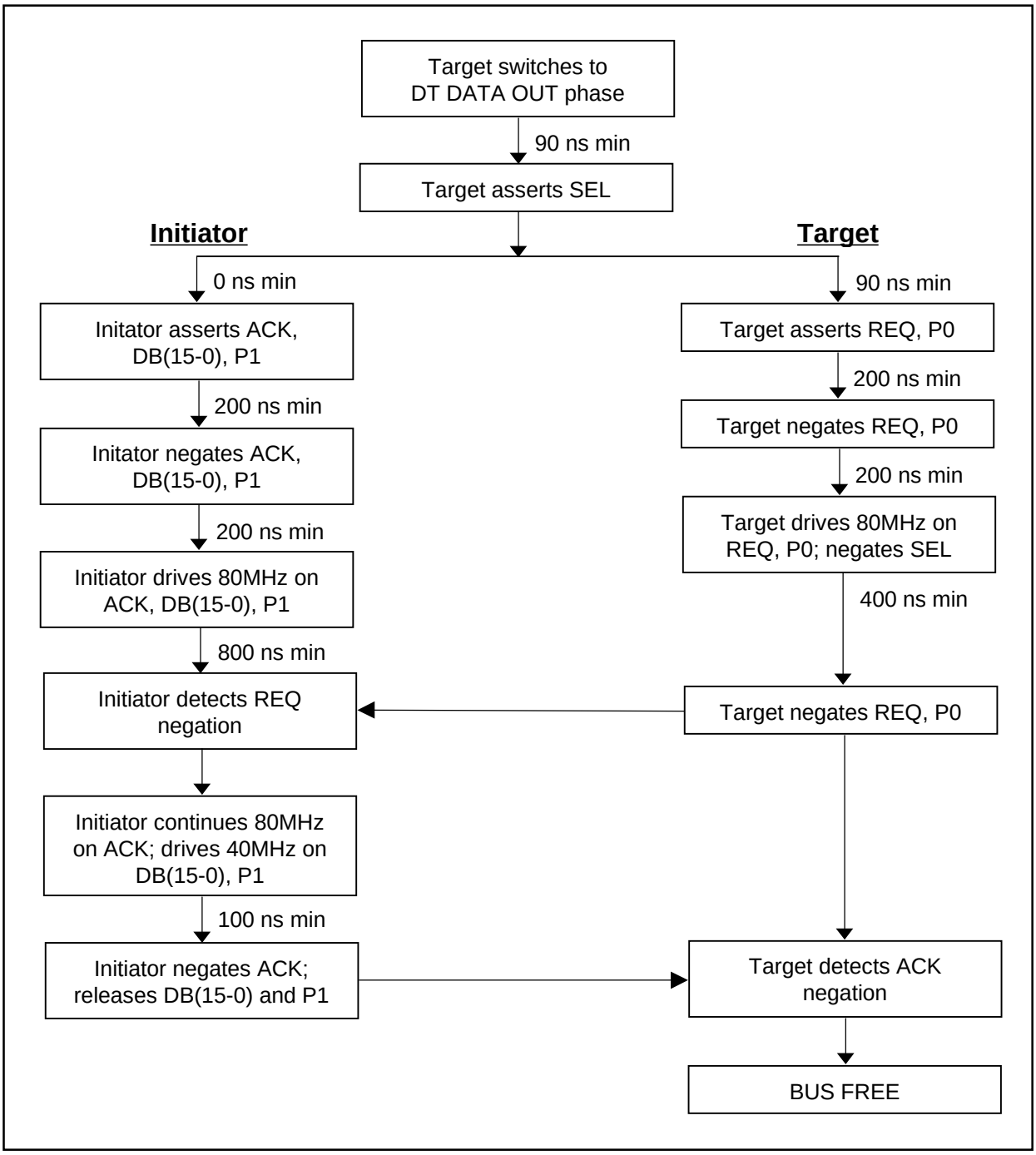

Figure x4 – Flow diagram for a DT DATA OUT training pattern after a DT DATA IN training pattern after a PARALLEL PROTOCOL REQUEST message

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16.3.10.1 PARALLEL PROTOCOL REQUEST message description

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Table 53 - PARALLEL PROTOCOL REQUEST message format

Bit / Byte	7	6	5	4	3	2	1	0
0	EXTENDED MESSAGE (01h)							
1	EXTENDED MESSAGE LENGTH (06h)							
2	PARALLEL PROTOCOL REQUEST (04h)							
3	TRANSFER PERIOD FACTOR							
4	RESERVED							
5	REQ/ACK OFFSET							
6	TRANSFER WIDTH EXPONENT (m)							
7	RESERVED			CAL_REQ		QAS_REQ	DT_REQ	IU_REQ

The PERIOD FACTOR field is defined in table 54.

Table 54 - TRANSFER PERIOD FACTOR field

Code	Description
00h-07h	Reserved (note 1)
08h	Transfer period equals 6,25 ns (note 2). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers and training patterns.
09h	Transfer period equals 12,5 ns (note 3). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.
0Ah	Transfer period equals 25 ns (note 4)
0Bh	Transfer period equals 30,3 ns (note 5)
0Ch	Transfer period equals 50 ns (note 5)
0Dh-18h	Transfer period equals the period factor x 4 (note 5)
19h-31h	Transfer period equals the period factor x 4 (note 6)
32h-FFh	Transfer period equals the period factor x 4 (note 7)

note:
1 - Faster timings may be allowed by future SCSI parallel interface standards.
2 - Fast-160 data is latched every 6,25 ns.
3 - Fast-80 data is latched every 12,5 ns.
4 - Fast-40 data is latched every 25 ns or 30,3 ns.
5 - Fast-20 data is latched using a transfer period of less than or equal 96 ns and greater than or equal to 50 ns.
6 - Fast-10 data is latched using a transfer period of less than or equal 196 ns and greater than or equal 100 ns.
7 - Fast-5 data is latched using a transfer period of less than or equal to 1 020 ns and greater than or equal to 200 ns.

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The protocol options bits (IU_REQ, DT_REQ, and QAS_REQ) and the CAL_REQ field are used by the initiator to indicate the protocol options to be enabled. The target uses the protocol options bits to indicate to the initiator if the requested protocol options are enabled. The target shall not enable any options that were not enabled in the PARALLEL PROTOCOL REQUEST message received from the initiator.

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If the Calibration support enable request bit (CAL_REQ) equals zero, the training pattern sequence shall not be initiated by the target. If the CAL_REQ bit equals one, the training pattern sequence may be initiated by the target. If the value in the TRANSFER PERIOD FACTOR field is less than or equal to 08h, then the CAL_REQ bit shall equal one.

Not all combinations of the protocol options bits are valid. Only the bit combinations defined in table 55 shall be allowed. All other combinations are reserved.

Table 55 - Valid protocol options bit combinations

CAL_REQ	QAS_REQ	DT_REQ	IU_REQ	Description
00b	0	0	0	Use ST DATA IN and ST DATA OUT phases to transfer data.
00b	0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers.
01b	0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers. The training pattern sequence is performed before every DATA IN and DATA OUT phase.
10b	0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers. The training pattern sequence is performed after every PARALLEL PROTOCOL REQUEST message.
00b	0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers.
01b	0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers. The training pattern sequence is performed before the first DATA IN and before the first DATA OUT phase of each nexus.
10b	0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers. The training pattern sequence is performed after every PARALLEL PROTOCOL REQUEST message.
00b	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration.
01b	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration. The training pattern sequence is performed before the first DATA IN and before the first DATA OUT phase of each nexus.
10b	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration. The training pattern sequence is performed after every PARALLEL PROTOCOL REQUEST message.