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Subject: Proposal for training pattern protocol to be included in SPI-4

Introduction

For parallel SCSI, skew compensation and equalization will be performed at the receiver on data and clock signals and equalization will be performed at the transmitter on clock signals in order to achieve the timings and signal quality required for transfer rates of 320 and 620 megabytes per second. This scheme could also be used to provide improved signal quality at lower transfer rates. In order to perform these operations, a specified training pattern must be sent by both the transmitter and receiver on specified signal lines during a specified time in a specified manner. The following is a proposal that defines the elements required for a training pattern.

The clauses referenced in this proposal are relative to the draft standard SCSI Parallel Interface – 3 (SPI-3) revision 13a. That document is available at ftp://ftp.t10.org/t10/drafts/spi3/spi3r13a.pdf.

4.9.3.x DT DATA phase training pattern and receiver calibration

The training pattern sequence provides for defined patterns to be transferred on data, clock, and data qualifier signals so that the receiver of the signals may perform skew compensation, equalization or other calibration operations to improve signal quality. The training pattern sequence is initiated by the target after entering a DT DATA phase before any data is transferred.

After a training pattern sequence is initiated for a DT DATA IN phase the target drives REQ, DB(15-0), P0, and P1 with the specified pattern. The initiator performs equalization on REQ, DB(15-0), P0, and P1. The initiator performs skew compensation on DB(15-0), P0, and P1. The initiator may also perform other operations on REQ, DB(15-0), P0, and P1 at this time. During this time the initiator drives ACK with the specified pattern. The target performs equalization and other operations on that signal.

After a training pattern sequence is initiated for a DT DATA OUT phase the initiator drives ACK, DB(15-0), and P1 with the specified pattern. The target performs equalization on ACK, DB(15-0), and P1. The target performs skew compensation on DB(15-0) and P1. The target may also perform other operations on REQ, DB(15-0), and P1 at this time. During this time the target drives REQ and P0 with the specified pattern. The initiator performs equalization and other operations on those signals.

Skew compensation, equalization, and other operations performed by the receiver to improve signal quality are vendor specific and not defined in this standard. See 10.8.3.3 for definition of the specific training pattern sequence.

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9.1 SCSI parallel bus timing values

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Table 29 - SCSI bus control timing values

Subclause	Timing description	Type	Description
	.....		
9.2.7	Bus settle delay	minimum	400 ns
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9.2.a	Training set up delay	minimum	200 ns
9.2.b	Training acknowledge delay	minimum	250 ns
9.2.c	First transmitter training time	minimum	1000 ns
9.2.d	Second transmitter training time	minimum	100 ns
9.2.e	Receiver training time	minimum	625 ns
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9.2.a Training set up delay

This time is used during the initiation of a training pattern sequence.

a) It is the minimum time that a target shall wait after asserting SEL before asserting REQ, DB(15-0), P0, and P1 at the beginning of a training pattern sequence during a DT DATA IN data phase.
b) It is the minimum time that a target shall wait after asserting SEL before asserting REQ and P0 for at the beginning of a training pattern sequence during a DT DATA OUT data phase.

9.2.b Training acknowledge delay

This time is used during acknowledgement of a training pattern sequence.

a) It is the minimum time that a target shall wait after asserting REQ, DB(15-0), P0, and P1 before negating REQ, DB(15-0), P0, and P1 at the beginning of a training pattern sequence during a DT DATA IN data phase.
b) It is the minimum time that a target shall wait after negating REQ, DB(15-0), P0, and P1 before beginning the first training pattern sequence during a DT DATA IN data phase.
c) It is the minimum time that an initiator shall wait after detecting the assertion of SEL before asserting ACK at the beginning of a training pattern sequence during a DT DATA IN data phase.
d) It is the minimum time that an initiator shall wait after asserting ACK before negating ACK at the beginning of a training pattern sequence during a DT DATA IN data phase.
e) It is the minimum time that an initiator shall wait after negating ACK before beginning a third training pattern sequence during a DT DATA IN data phase.
f) It is the minimum time that an initiator shall wait after detecting the assertion of SEL before asserting before asserting ACK, DB(15-0), and P1 at the beginning of a training pattern sequence during a DT DATA OUT data phase.

g) It is the minimum time that an initiator shall wait after asserting ACK, DB(15-0), and P1 before negating ACK, DB(15-0), and P1 at the beginning of a training pattern sequence during a DT DATA OUT data phase.
h) It is the minimum time that an initiator shall wait after negating ACK, DB(15-0), and P1 before beginning a first training pattern sequence during a DT DATA OUT data phase.
i) It is the minimum time that a target shall wait after asserting REQ and P0 before negating REQ and P0 at the beginning of a training pattern sequence during a DT DATA OUT data phase.
j) It is the minimum time that a target shall wait after negating REQ and P0 before beginning of a third training pattern sequence during a DT DATA OUT data phase.

9.2.c First transmitter training time

This is the minimum time that a target or initiator transmits training pattern 1 (see 10.8.3.3).

9.2.d Second transmitter training time

This is the minimum time that a target or initiator transmits training pattern 2 (see 10.8.3.3).

9.2.e Receiver training time

This is the minimum time that a target or initiator transmits training pattern 3 (see 10.8.3.3).

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10.8.3.3.x DT DATA IN phase training pattern sequence

The target shall not initiate a training pattern sequence until at least one bus settle delay after the beginning of a DT DATA IN phase. The target shall initiate a training pattern sequence by asserting SEL. After asserting SEL, the target shall wait at least one training set up delay and then assert REQ, DB(15-0), P0, and P1. The target shall wait at least one training acknowledge delay and then negate REQ, DB(15-0), P0, and P1.

After negating REQ, DB(15-0), P0, and P1, the target shall wait at least one training acknowledge delay and then begin alternately asserting and negating REQ every (transfer period ÷ 2) ns (i.e., an alternating "101010..." pattern) and transmit the first training pattern by alternately asserting and negating DB(15-0), P0, and P1 every (transfer period ÷ 2) ns for at least one first transmitter training time. Assertion and negation of REQ, DB(15-0), P0, and P1 shall be in phase.

The target may negate SEL one training pattern acknowledge delay after beginning the alternate assertion and negation of REQ, DB(15-0), P0, and P1.

After transmitting the first training pattern for at least one first transmitter training time, the target shall transmit the second training pattern by alternately asserting and negating DB(15-0), P0, and P1 every (transfer period) ns (i.e., an alternating "110011001100..." pattern) for at least one second transmitter training time. Assertion and negation of REQ, DB(15-0), P0, and P1 shall be in phase.

After transmitting the second training pattern for at least one second transmitter training time, the target shall negate DB(15-0), P0, and for at least (transfer period × 2) ns. After negating DB(15-0), P0, and P1 for at least (transfer period × 2) ns, the target may begin transmitting data for the phase.

After detecting the assertion of SEL, the initiator shall wait at least one training set up delay and then assert ACK. After asserting ACK the initiator shall wait at least one training acknowledge delay and then negate ACK. After negating ACK, the target shall transmit a training pattern by alternately asserting and negating ACK every (transfer period ÷ 2) ns (i.e., an alternating "101010..." pattern) for at least one

receiver training time. After alternately asserting and negating ACK for at least one receiver training time, the initiator shall negate ACK.

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10.8.3.3.y DT DATA OUT phase training pattern sequence

The target shall not initiate a training pattern sequence until at least one bus settle delay after the beginning of a DT DATA IN phase. The target shall initiate a training pattern sequence by asserting SEL. After asserting SEL, the target shall wait at least one training set up delay and then assert REQ and P0. After asserting REQ and P0, the target shall wait at least one training acknowledge delay and then negate REQ and P0.

After negating REQ and P0, the target shall wait one training acknowledge delay and then transmit a training pattern by alternately asserting and negating REQ and P0 every (transfer period ÷ 2) ns for at least one receiver training time. After alternately asserting and negating REQ and P0 for at least one receiver training time, the target shall negate REQ and P0. The target may negate SEL one training pattern acknowledge delay after beginning the alternate assertion and negation of REQ and P0.

After detecting the assertion of SEL, the initiator shall wait at least one training set up delay and then assert ACK, DB(15-0), and P1. After asserting ACK, DB(15-0), and P1, the initiator shall wait at least one training acknowledge delay and then negate ACK, DB(15-0), and P1.

After negating ACK, DB(15-0), and P1, the initiator shall wait at least one training acknowledge delay and then begin alternately asserting and negating ACK every (transfer period ÷ 2) ns and transmit the first training pattern by alternately asserting and negating DB(15-0) and P1 every (transfer period ÷ 2) ns for at least one training pattern time. Assertion and negation of ACK, DB(15-0), and P1 shall be in phase.

After transmitting the first training pattern for at least one first transmitter time, the initiator shall transmit the second training pattern by alternately asserting and negating DB(15-0) and P1 every (transfer period) ns for at least one second transmitter training time. Assertion and negation of ACK, DB(15-0), and P1 shall be in phase. After transmitting the second training pattern for at least one second transmitter training time, the initiator shall negate DB(15-0), and P1 for at least (transfer period × 2) ns.

After detecting that P1 has been negated for at least (transfer period × 2) ns, the target may begin transmitting REQ pulses for the data phase.

The initiator may begin transferring data for the phase as soon as REQ pulses are detected from the target.

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16.3.10.1 PARALLEL PROTOCOL REQUEST message description

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Table 53 - PARALLEL PROTOCOL message format

Bit / Byte	7	6	5	4	3	2	1	0
0	EXTENDED MESSAGE (01h)							
1	EXTENDED MESSAGE LENGTH (06h)							
2	PARALLEL PROTOCOL REQUEST (04h)							
3	TRANSFER PERIOD FACTOR							
4	RESERVED							
5	REQ/ACK OFFSET							
6	TRANSFER WIDTH EXPONENT (m)							
7	RESERVED				CAL_REQ	QAS_REQ	DT_REQ	IU_REQ

The PERIOD FACTOR field is defined in table 54.

Table 54 - TRANSFER PERIOD FACTOR field

Code	Description
00h-07h	Reserved (note 1)
08h	Transfer period equals 6,25 ns (note 2). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers and training patterns.
09h	Transfer period equals 12,5 ns (note 3). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.
0Ah	Transfer period equals 25 ns (note 4)
0Bh	Transfer period equals 30,3 ns (note 5)
0Ch	Transfer period equals 50 ns (note 5)
0Dh-18h	Transfer period equals the period factor x 4 (note 5)
19h-31h	Transfer period equals the period factor x 4 (note 6)
32h-FFh	Transfer period equals the period factor x 4 (note 7)

note:
1 - Faster timings may be allowed by future SCSI parallel interface standards.
2 - Fast-160 data is latched every 6,25 ns.
3 - Fast-80 data is latched every 12,5 ns.
4 - Fast-40 data is latched every 25 ns or 30,3 ns.
5 - Fast-20 data is latched using a transfer period of less than or equal 96 ns and greater than or equal to 50 ns.
6 - Fast-10 data is latched using a transfer period of less than or equal 196 ns and greater than or equal 100 ns.
7 - Fast-5 data is latched using a transfer period of less than or equal to 1 020 ns and greater than or equal to 200 ns.

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The protocol options bits (IU_REQ, DT_REQ, QAS_REQ, and CAL_REQ) are used by the initiator to indicate the protocol options to be enabled. The target uses the protocol options bits to indicate to the initiator if the requested protocol options are enabled. The target shall not enable any options that were not enabled in the PPR message received from the initiator.

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If the Calibration support enable request bit (CAL_REQ) equals zero, the training pattern sequence shall not be initiated by the target. If the CAL_REQ bit equals one, the training pattern sequence may be initiated by the target. If the value in the TRANSFER PERIOD FACTOR field is less than or equal to 08h, then the CAL_REQ bit shall equal one.

Not all combinations of the protocol options bits are valid. Only the bit combinations defined in table 55 shall be allowed. All other combinations are reserved.

Table 55 - Valid protocol options bit combinations

CAL_REQ	QAS_REQ	DT_REQ	IU_REQ	Description
0	0	0	0	Use ST DATA IN and ST DATA OUT phases to transfer data.
0	0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers.
1	0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers. The training pattern sequence may be used.
0	0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers.
1	0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers. The training pattern sequence may be used.
0	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration.
1	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration. The training pattern sequence may be used.