# SCSI Connector and Cable Modeling from TDR Measurements

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**Presented at SCSI Signal Modeling Study Group**

**Rochester, MN, December 1, 1999**

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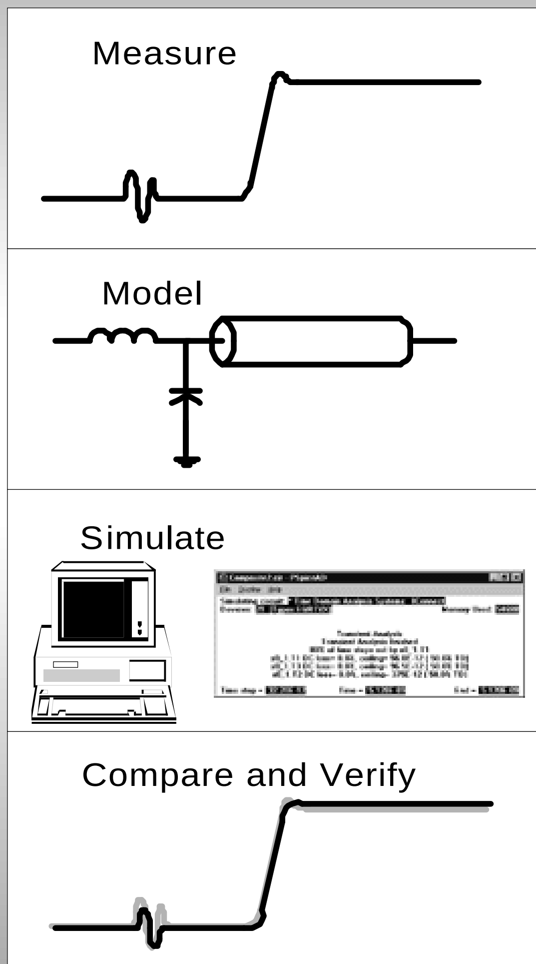
# Outline

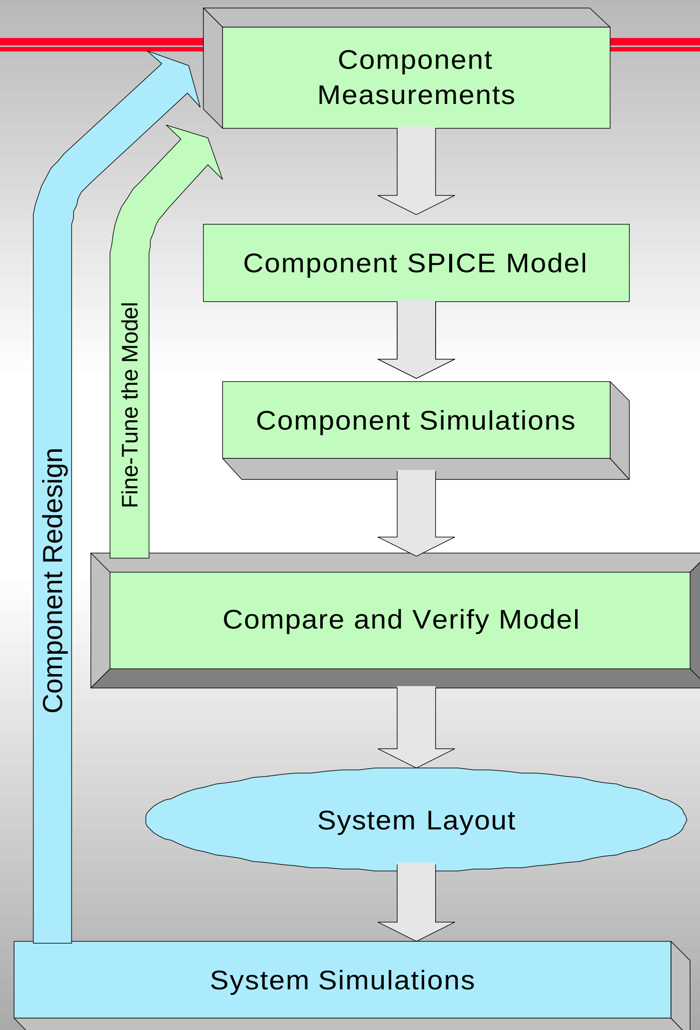
- ☛ **Interconnect Modeling Methodology**
- **Single-Ended TDR Modeling**
  - **TDR Basics**
  - **REQ Signal Model**
- **Differential TDR Modeling**
  - **TDR Basics**
  - **REQ Signal Model**

# Signal Integrity Modeling

- **Goal: create SPICE models to predict connector/cable performance**
- **Model *required range of validity* is defined by a greater of**
  - **signal rise time: $f_{bw}=0.35 / t_{rise}$**
  - **signal clock rate: $f_{bw}= (3\sim5) \cdot f_{clock}$**
- **It may be desired to extend the required range of model validity beyond $f_{bw}$**

# Measurement Based Approach

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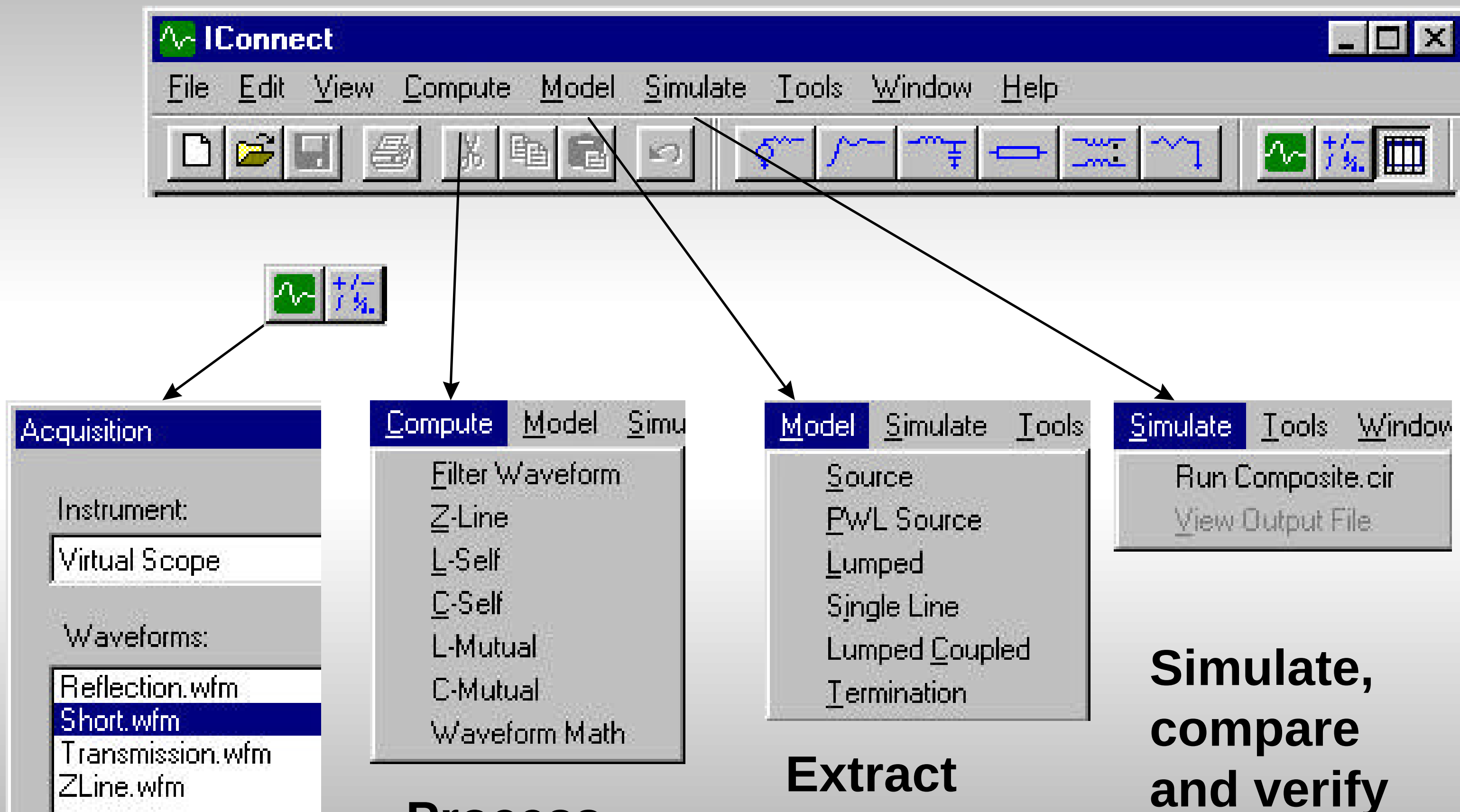
# IConnect™ Modeling Process




**Measure and acquire**

**Process data**

**Extract model**

**Simulate, compare and verify**

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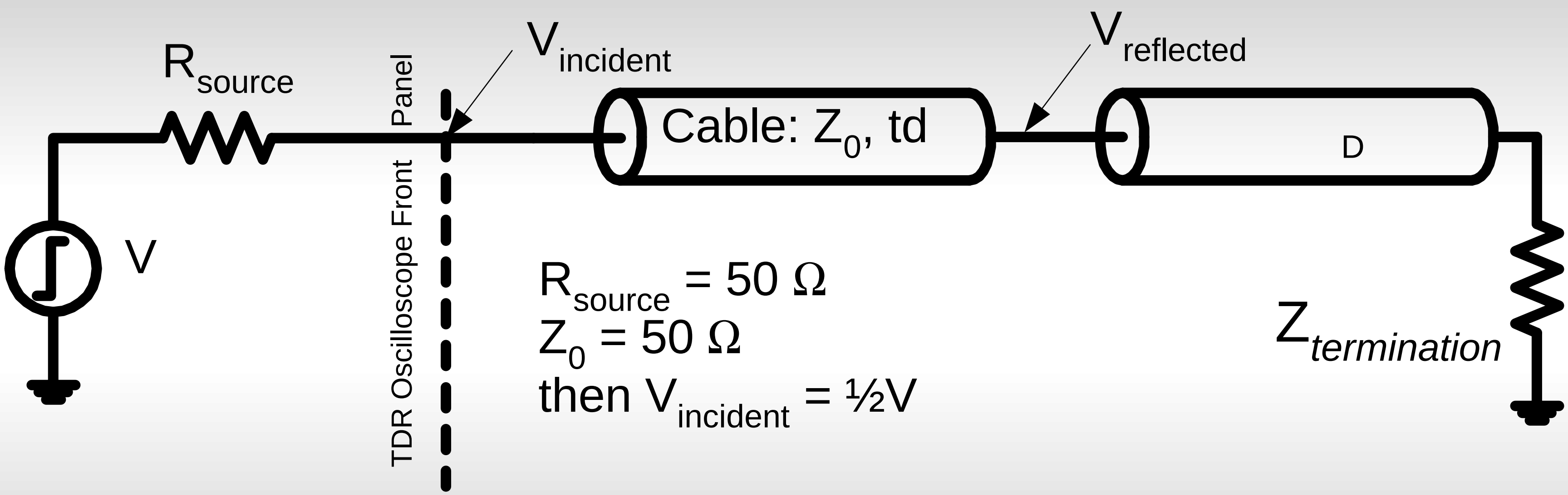
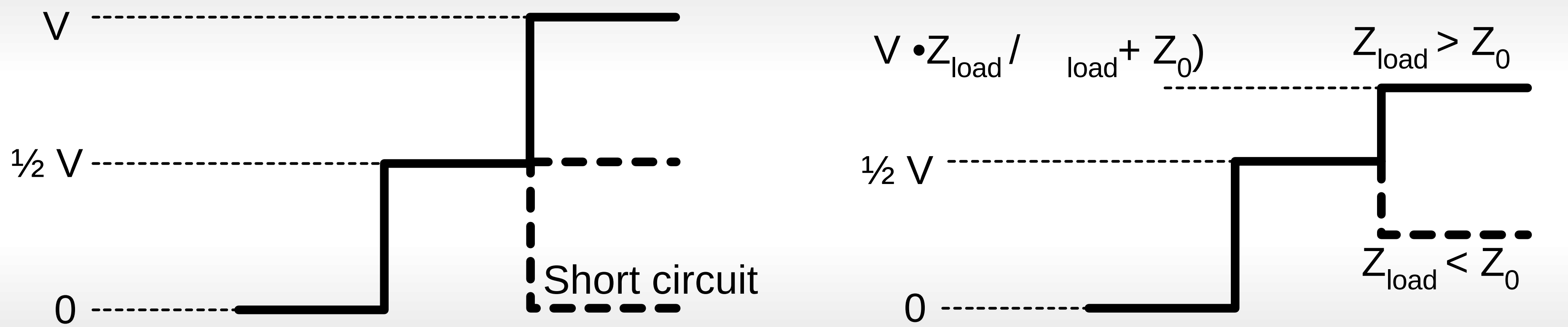
- Differential TDR Modeling
  - TDR Basics
  - REQ Signal Model

# TDR Block Diagram

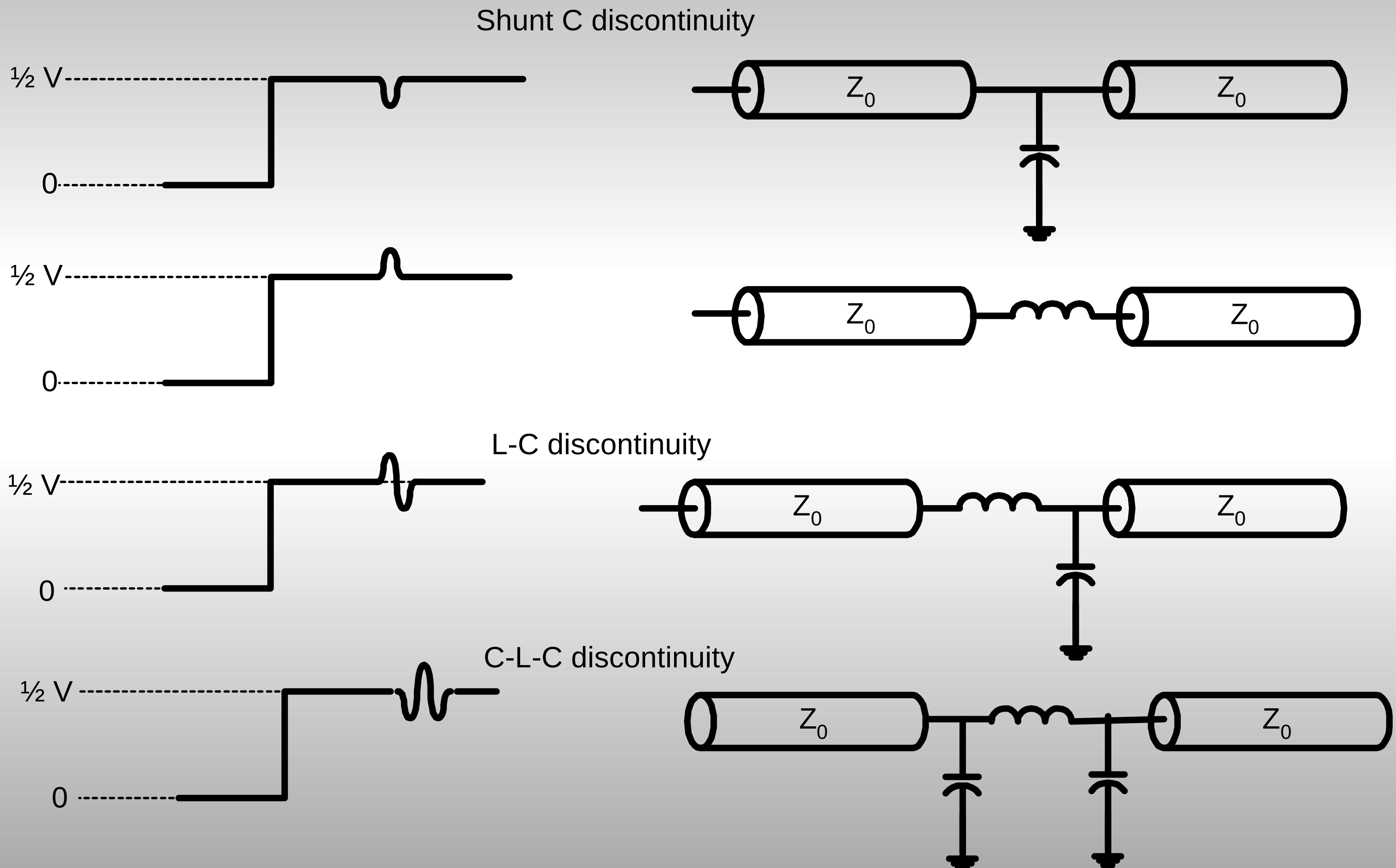



**Note: TDR source may actually be implemented as a Norton equivalent current source**

# TDR Visual Representation



# Inductance and Capacitance Analysis

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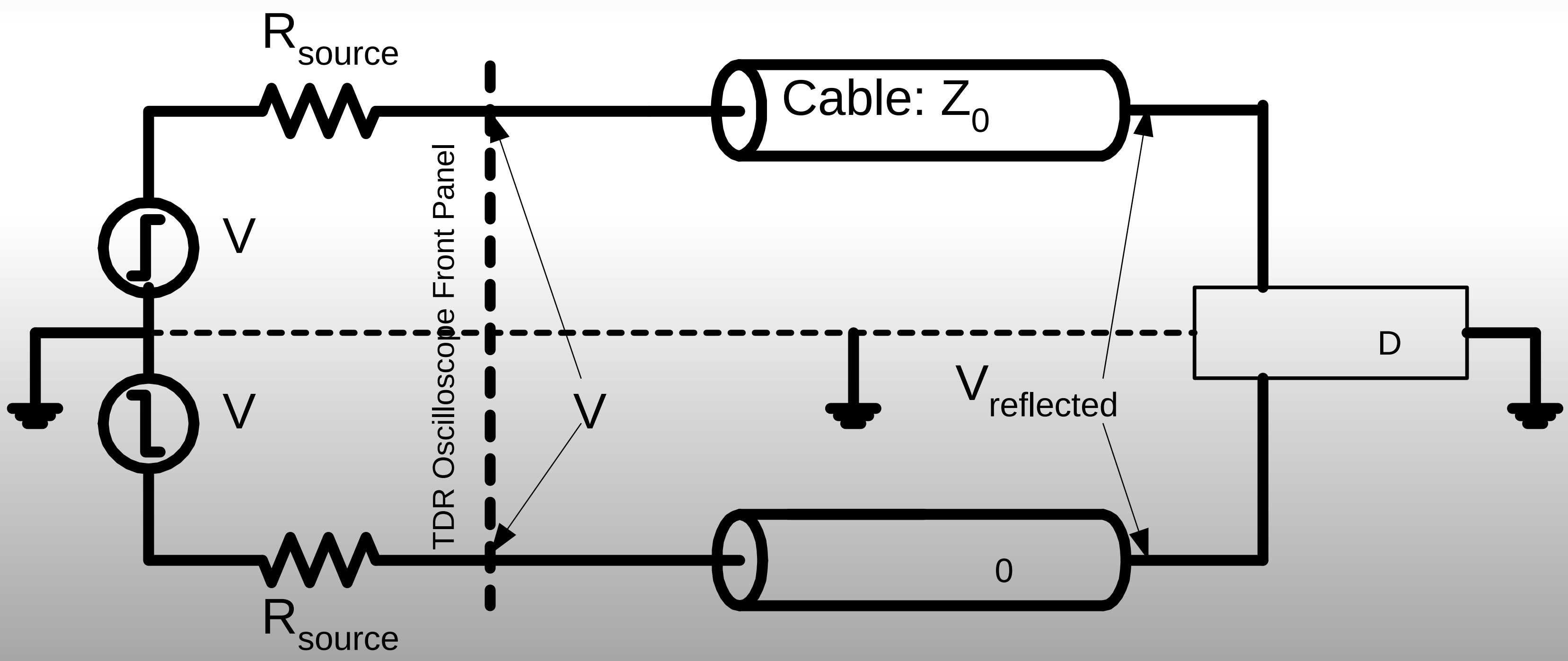
# Differential TDR

- Virtual ground plane
- Even and odd mode measurements

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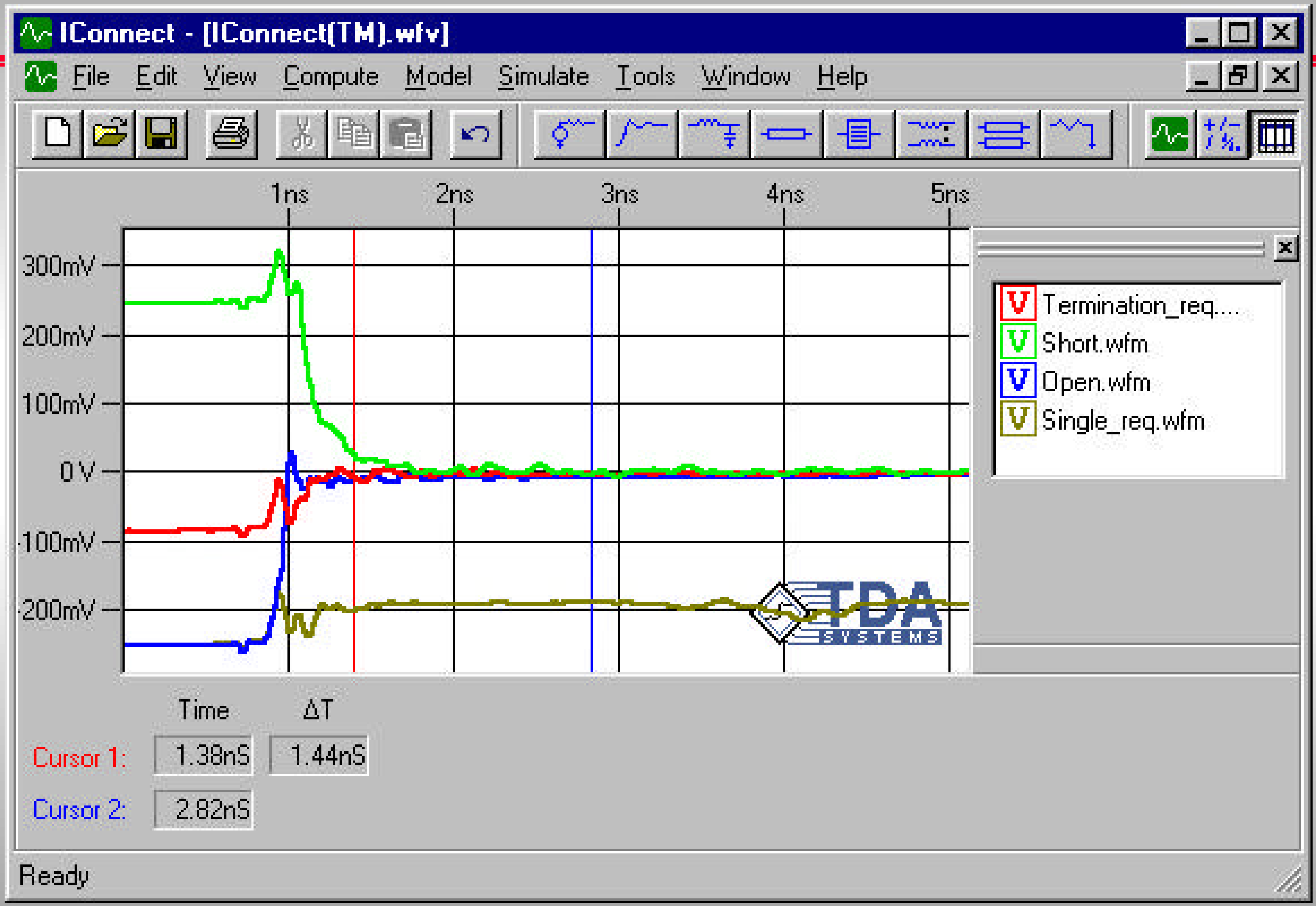
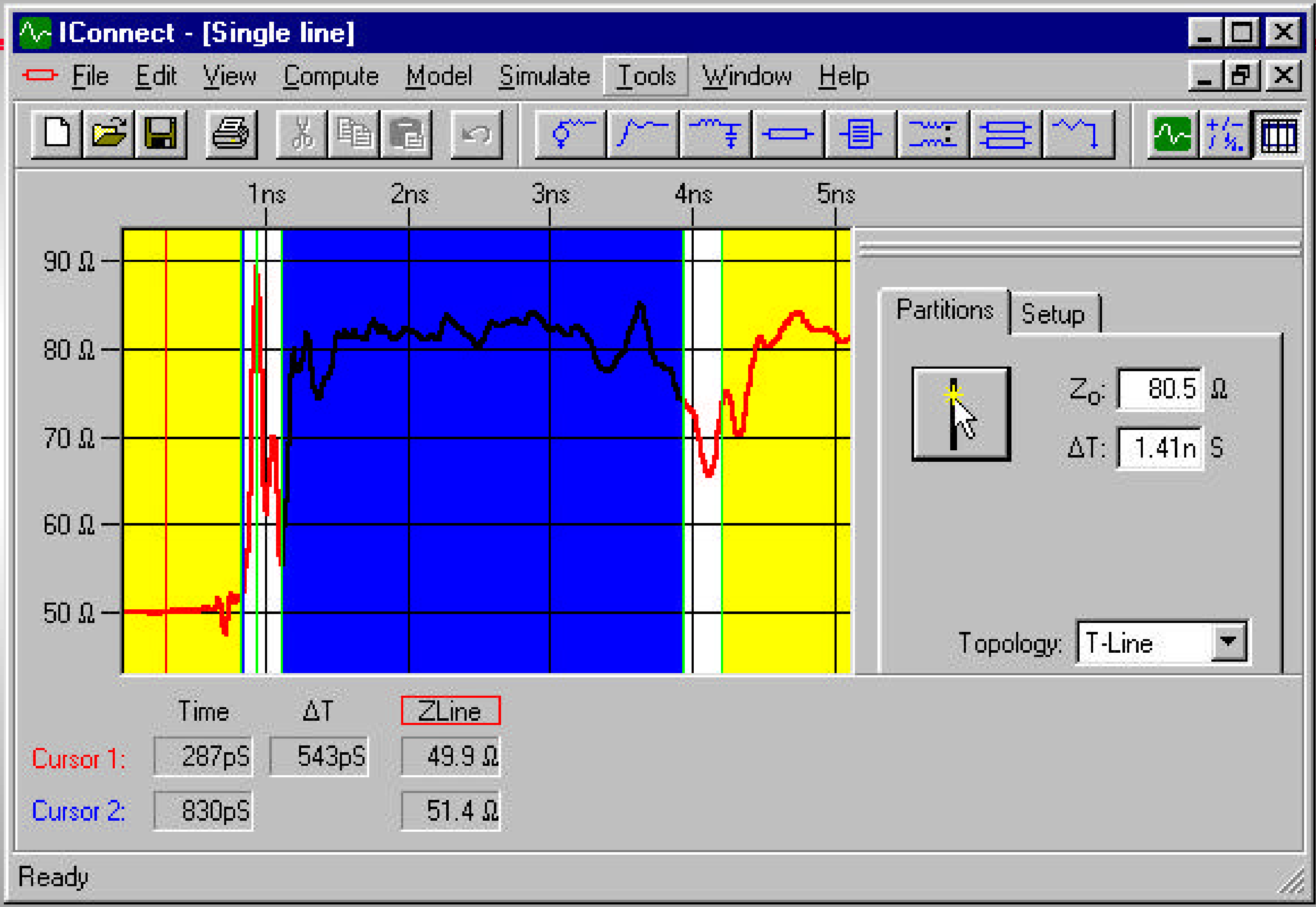
# REQ: Acquire Waveforms



# Partition Impedance Profile and Create a Model



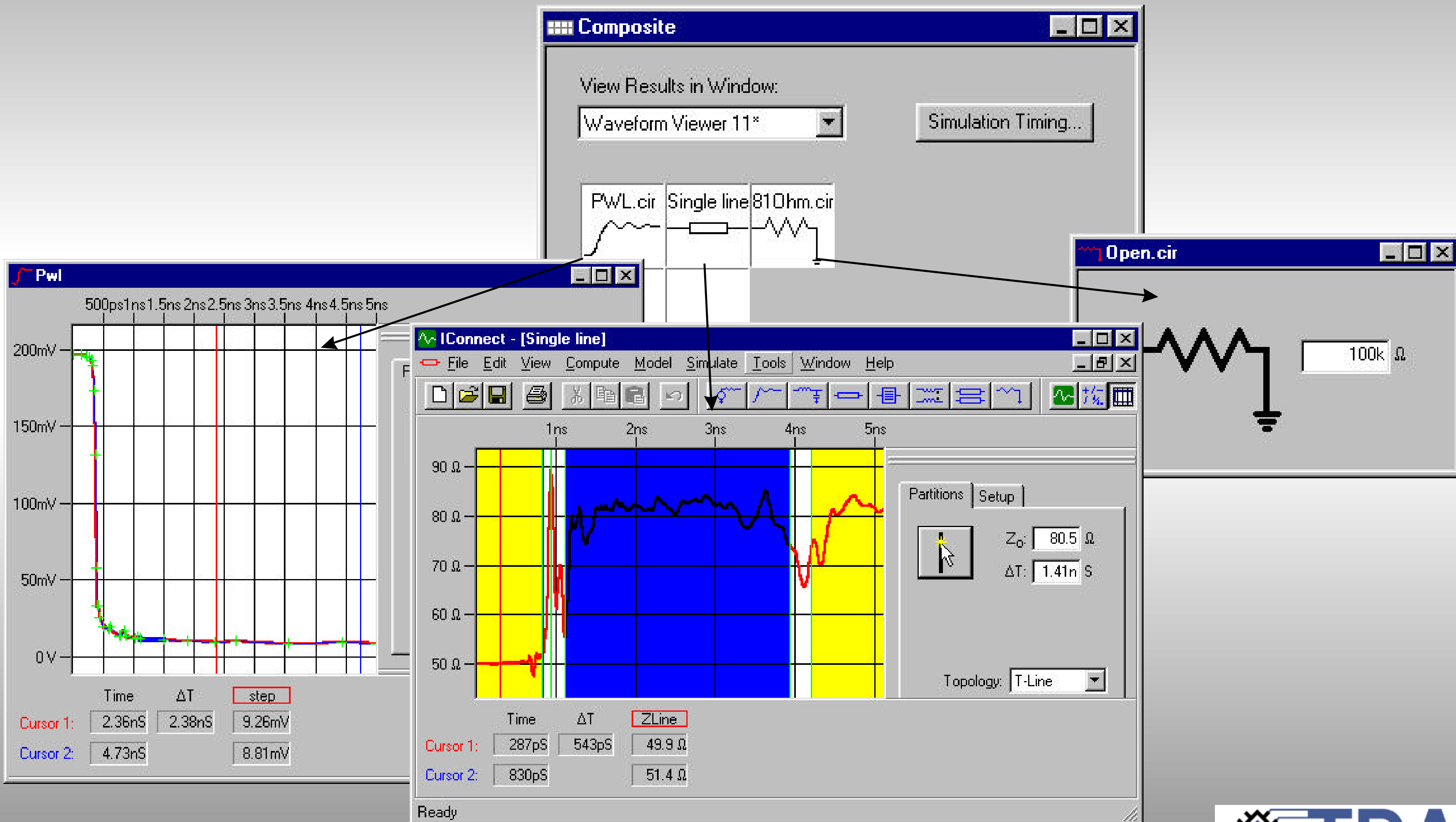
# Model Listing

Connector

Cable

```
****** Partition #1
   l1  1  4 3.54n
****** Partition #2
   c1  4  3 1p
   l2  4  5 1n
****** Partition #3
   t1  5  3  6  3
Z0=80.5 TD=1.41n
****** Partition #4
   t2  6  3  2  3 Z0=65.5 TD=143p
```

# Composite Model Generation

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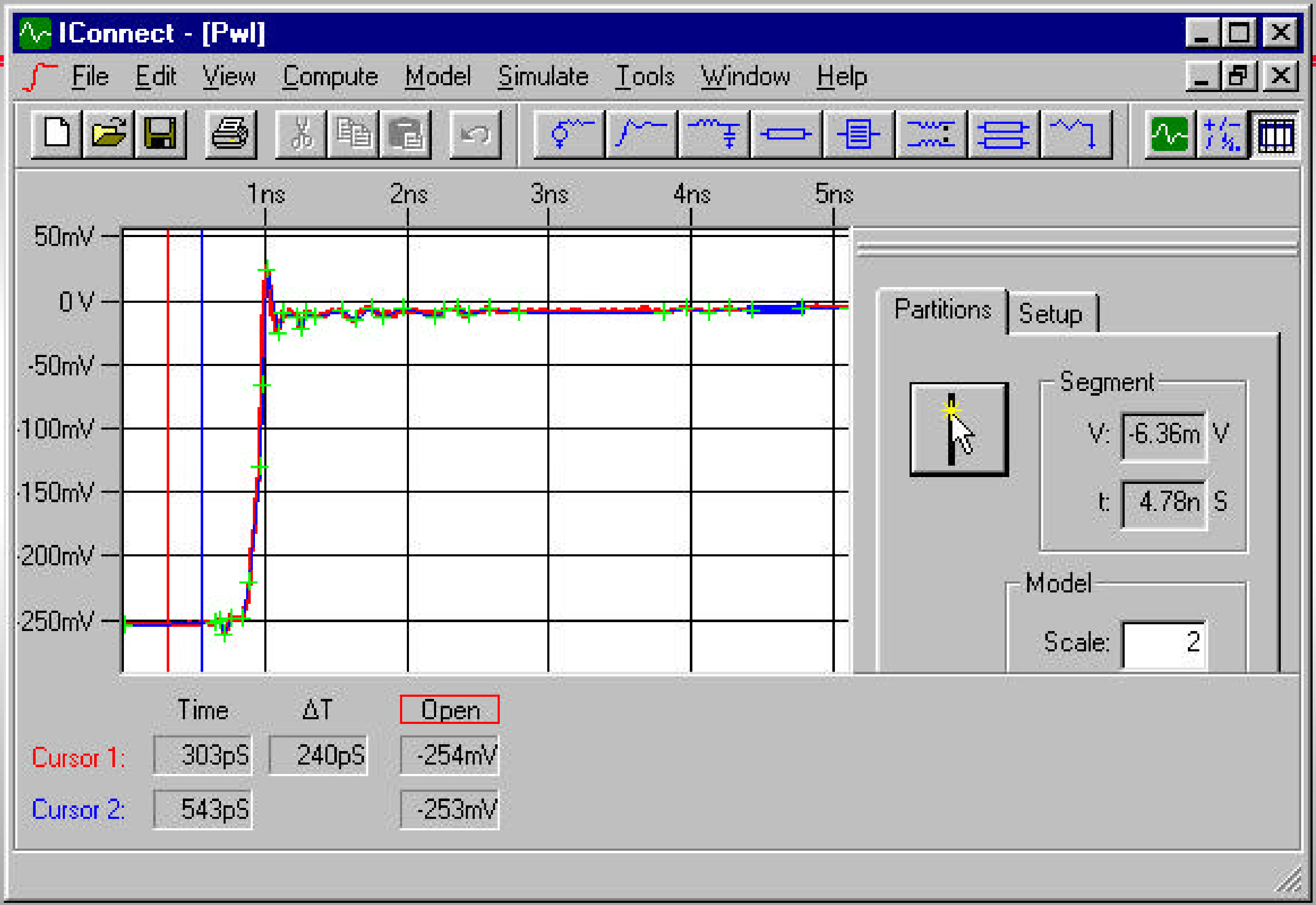
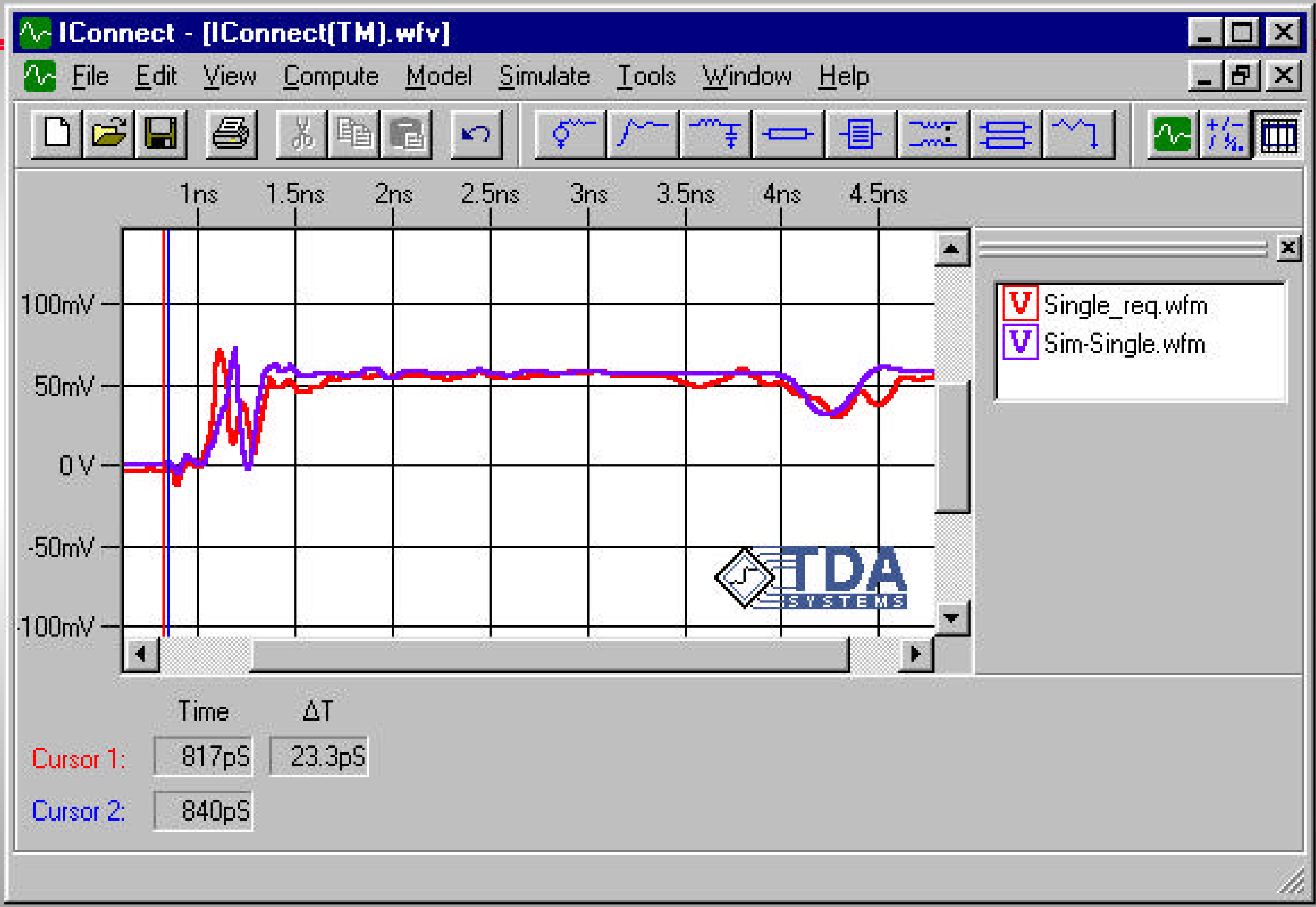
# Create Piecewise Linear Source



# Simulate and Verify

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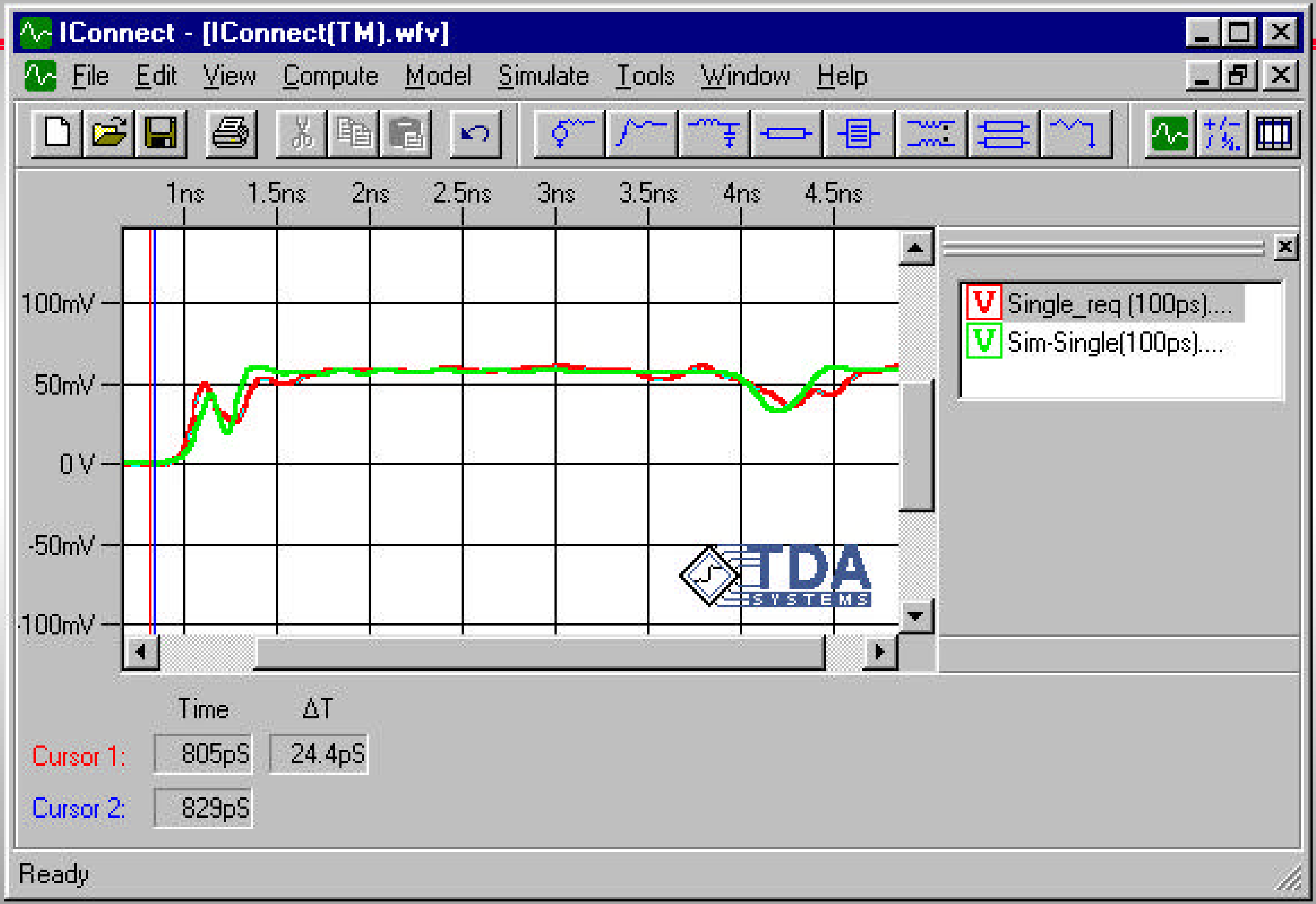
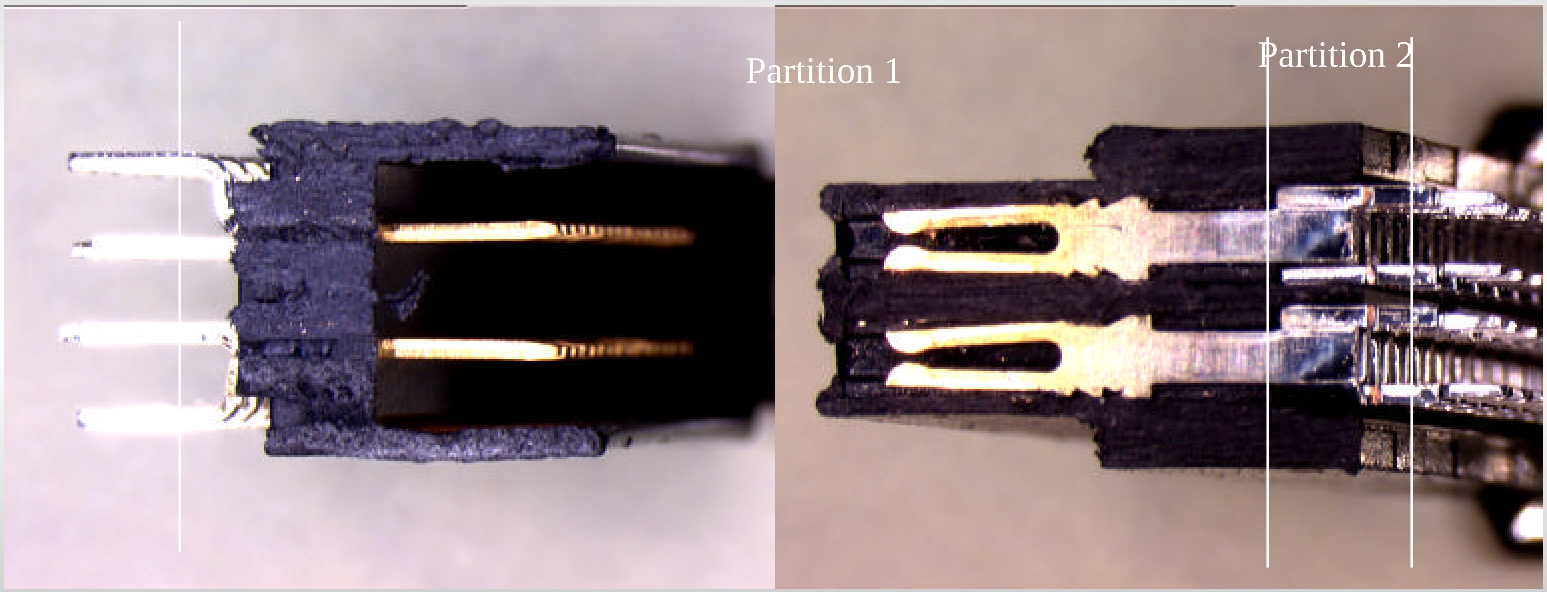
# User Rise Time Filtering to Achieve Simple Models



# Correlation to Physical Structure

PCB section

Cable section



# Outline

- ✓ **Interconnect Modeling Methodology**
- ✓
  - **TDR Basics**
  -
- ☛ **Differential TDR Modeling**
  -
  - **REQ Signal Model**

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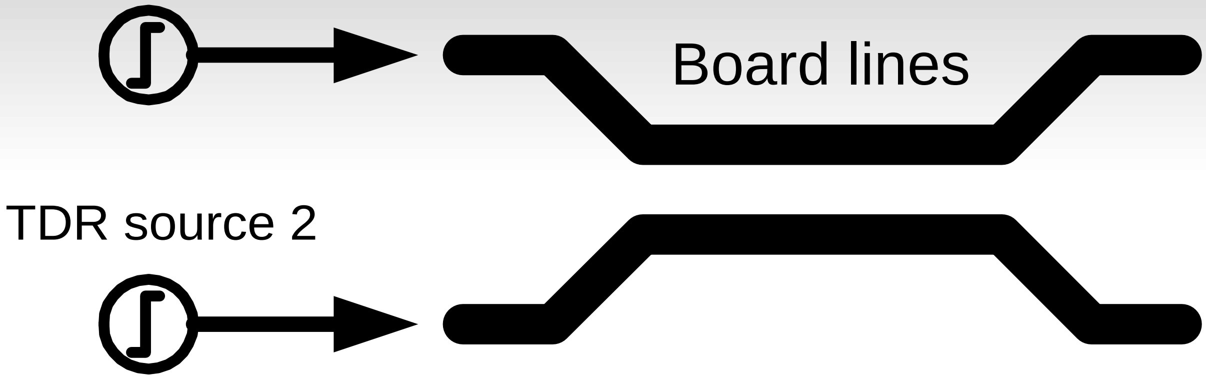
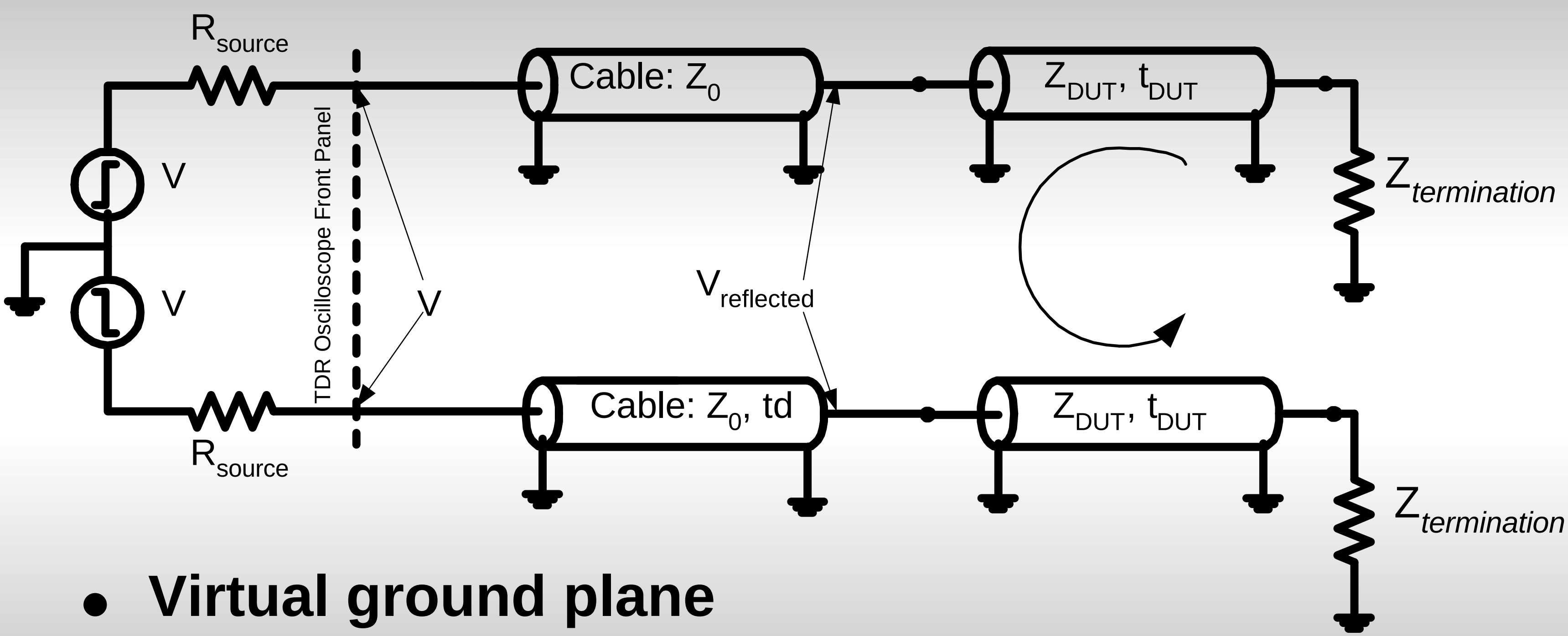
# Symmetrical Coupled Line Model



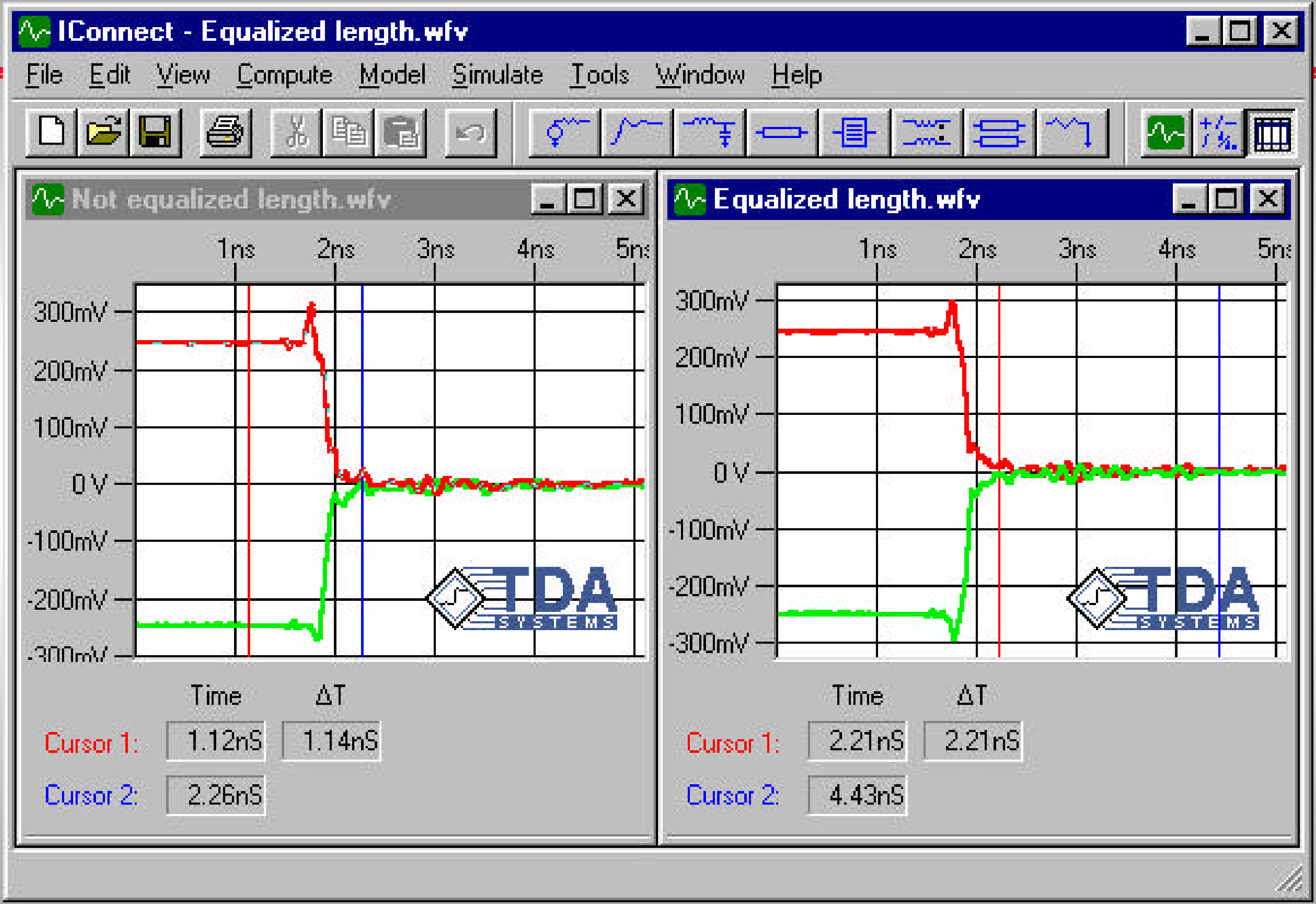

- **Assumptions:**
  - **the lines are symmetrical**
  - **TDR pulses are symmetrical**
  - **TDR pulses arrive at the lines at the same time at the beginning of both lines**

# Differential TDR Measurement Setup




- **Virtual ground plane**
- **Assumptions:**
  - **Lines under test (DUT) are symmetrical**
  - **TDR pulses are symmetrical**
  - **TDR pulses arrive at the DUT at the same time**

# Equalize the TDR Delay




- **Watch for the symmetry in the traces rather than relative position in time**

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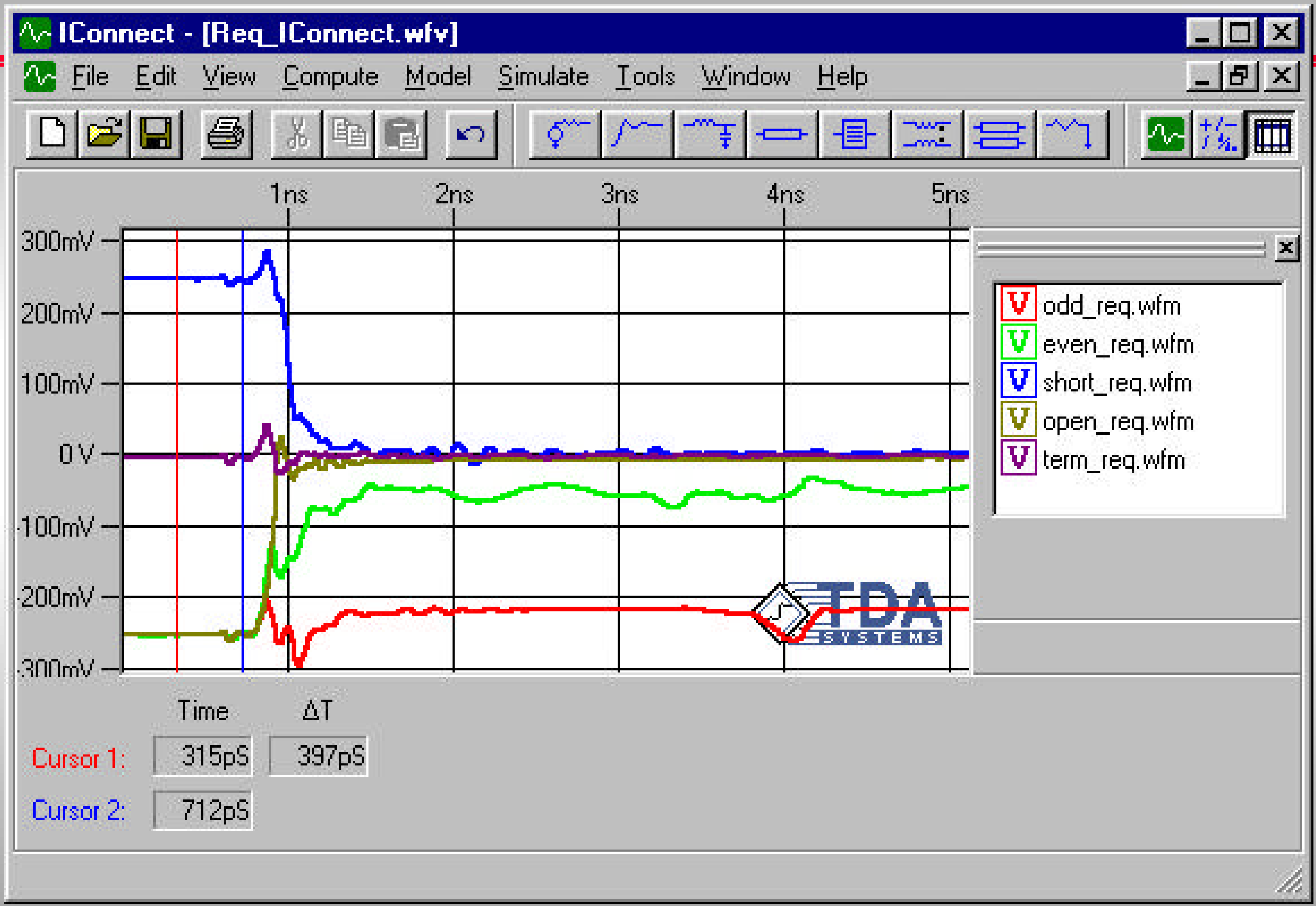
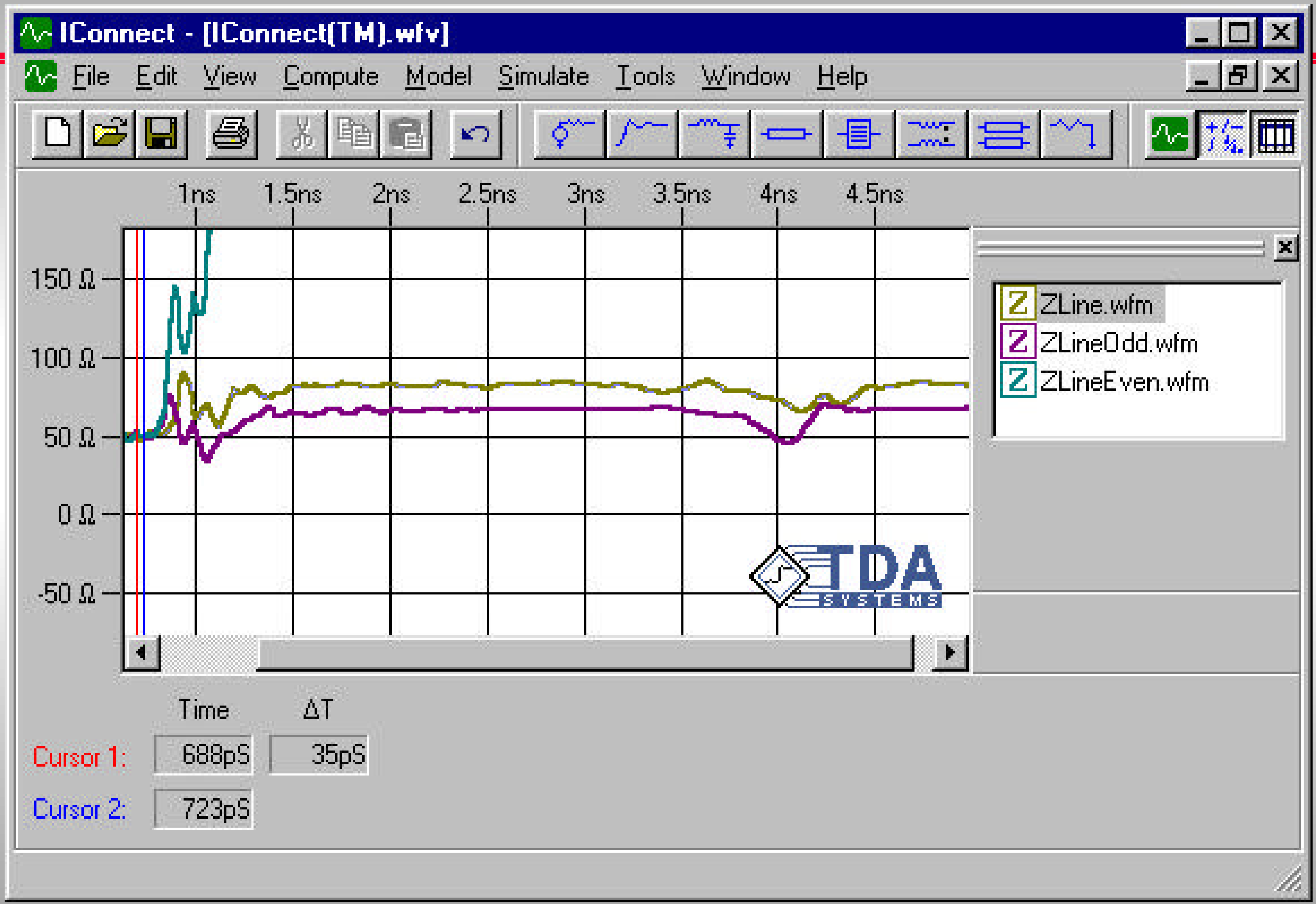
# Acquire Waveforms



# Single Line Impedance vs. Odd and Even

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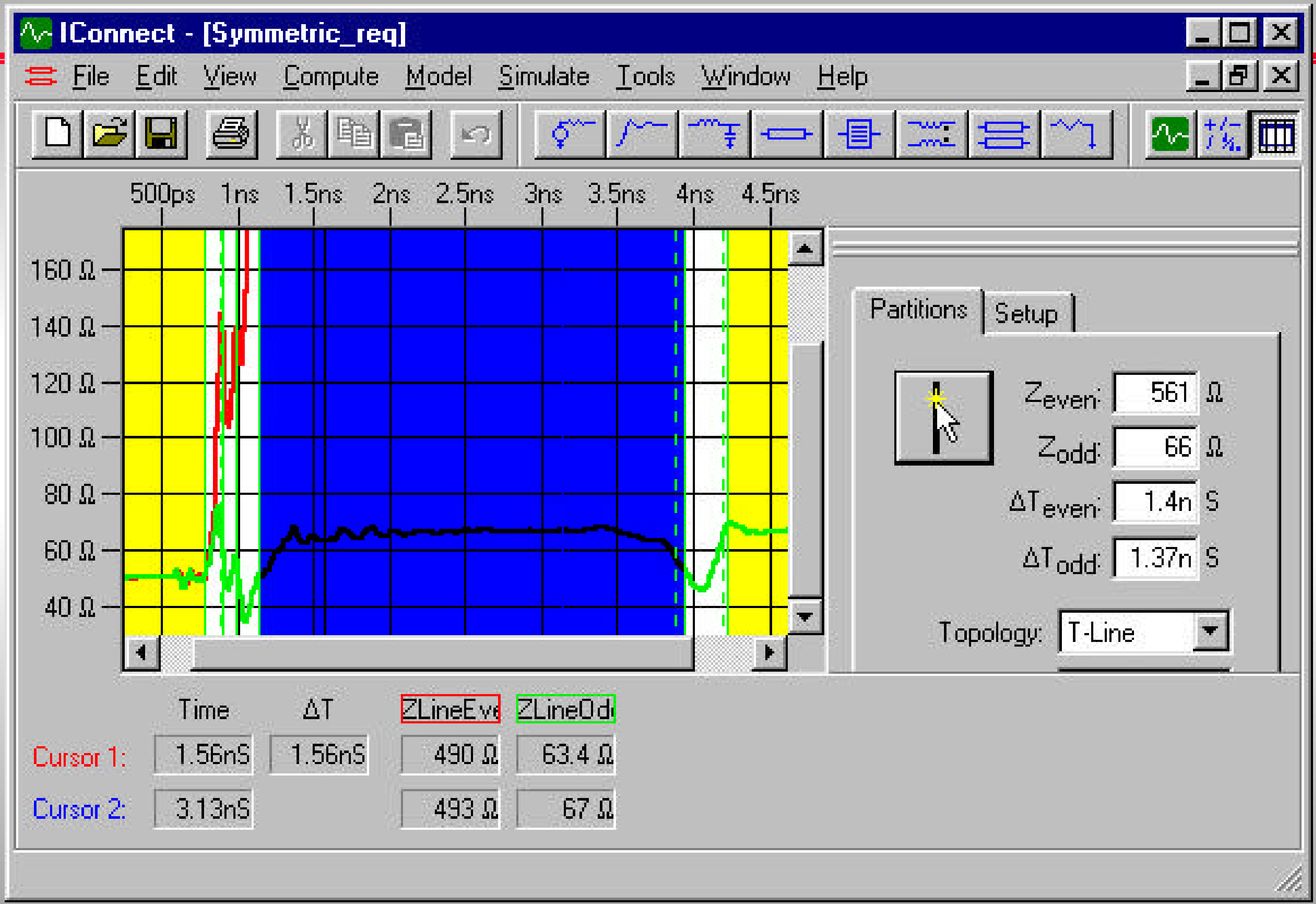
# Create a Model

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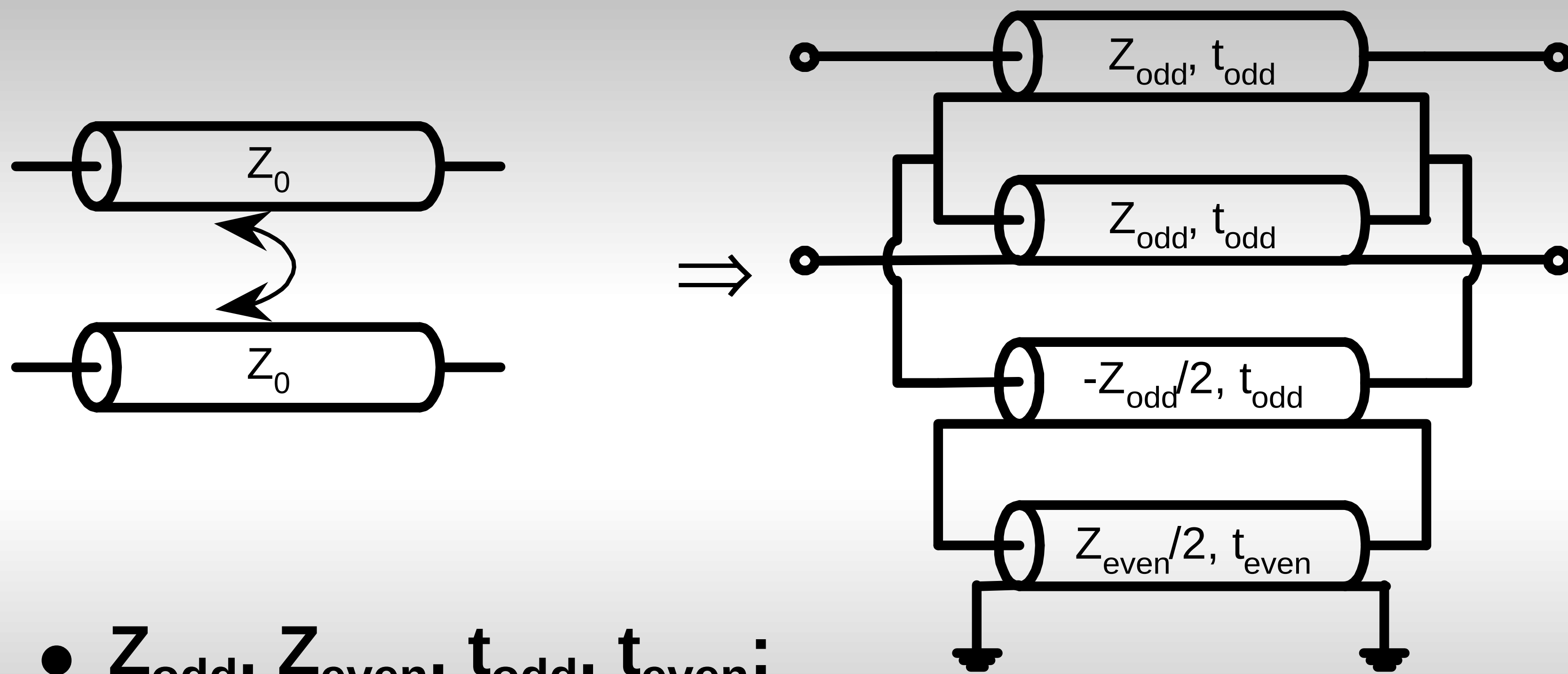
# Symmetrical Coupled Line Model

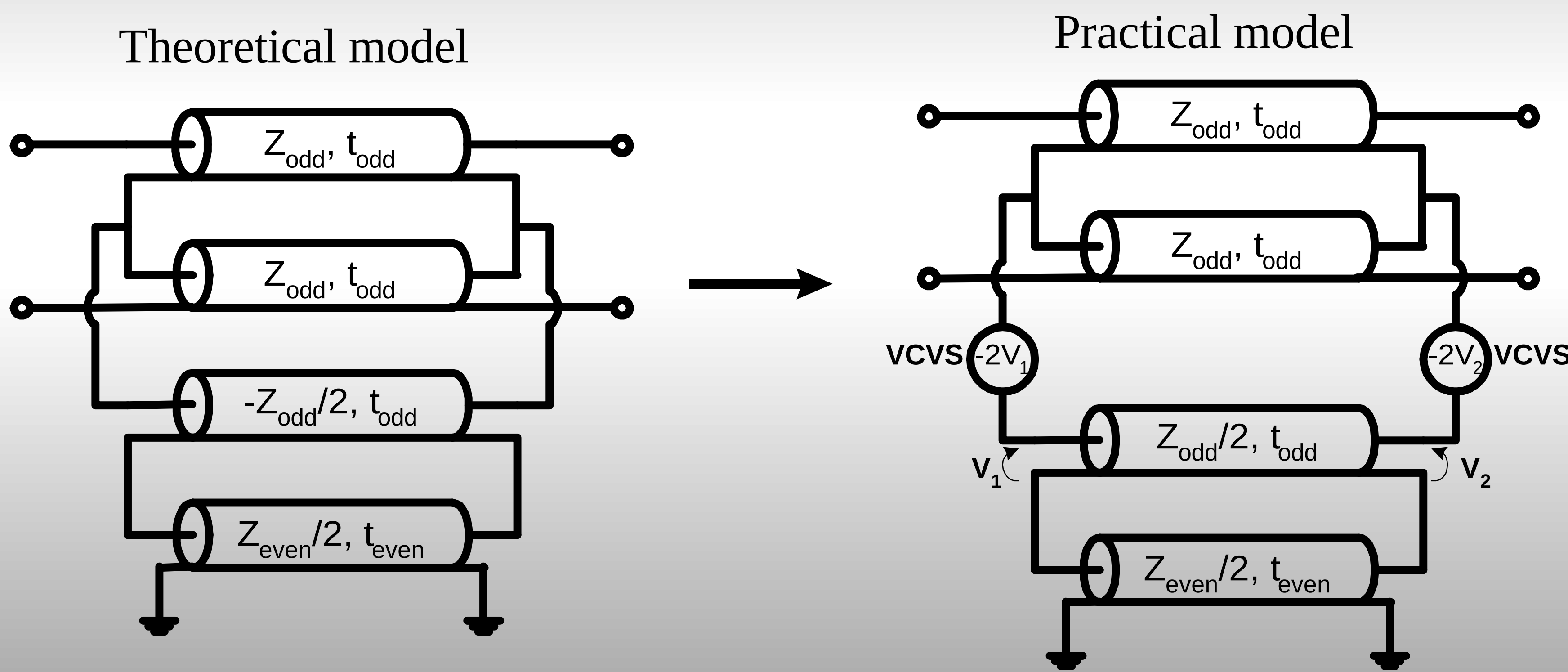



- **$Z_{odd}$, $Z_{even}$, $t_{odd}$, $t_{even}$:**

  **directly obtained from odd and even impedance profiles**

# Practical Model Output

- To avoid negative Z in theoretical model:



# Model Listing

Connectors

****** Partition #1

l1  1  6 4n

c1  6  5 710f

l2  3  7 4n

c2  7  5 710f

c3  6  7 33.7f

k1 l1 l2 226m

****** Partition #2

t1  6  8  9  10 Z0=51.4 TD=43.5p

t2  7  8  11  10 Z0=51.4 TD=43.5p

e1  12  8  12  13 2

e2  14  10  14  15 2

t3  12  13  14  15 Z0=25.7 TD=43.5p

t4  13  5  15  5 Z0=58.5 TD=44.5p

****** Partition #3

c4  9  5 423f

l3  9  16 7.96n

c5  11  5 423f

l4  11  17 7.96n

c6  9  11 643f

k2 l3 l4 603m

Cables

****** Partition #4

t5  16  18  19  20 Z0=66 TD=1.37n

t6  17  18  21  20 Z0=66 TD=1.37n

e3  22  18  22  23 2

e4  24  20  24  25 2

t7  22  23  24  25 Z0=33 TD=1.37n

t8  23  5  25  5 Z0=281 TD=1.4n

****** Partition #5

t9  19  26  2  27 Z0=45.7 TD=125p

t10  21  26  4  27 Z0=45.7 TD=125p

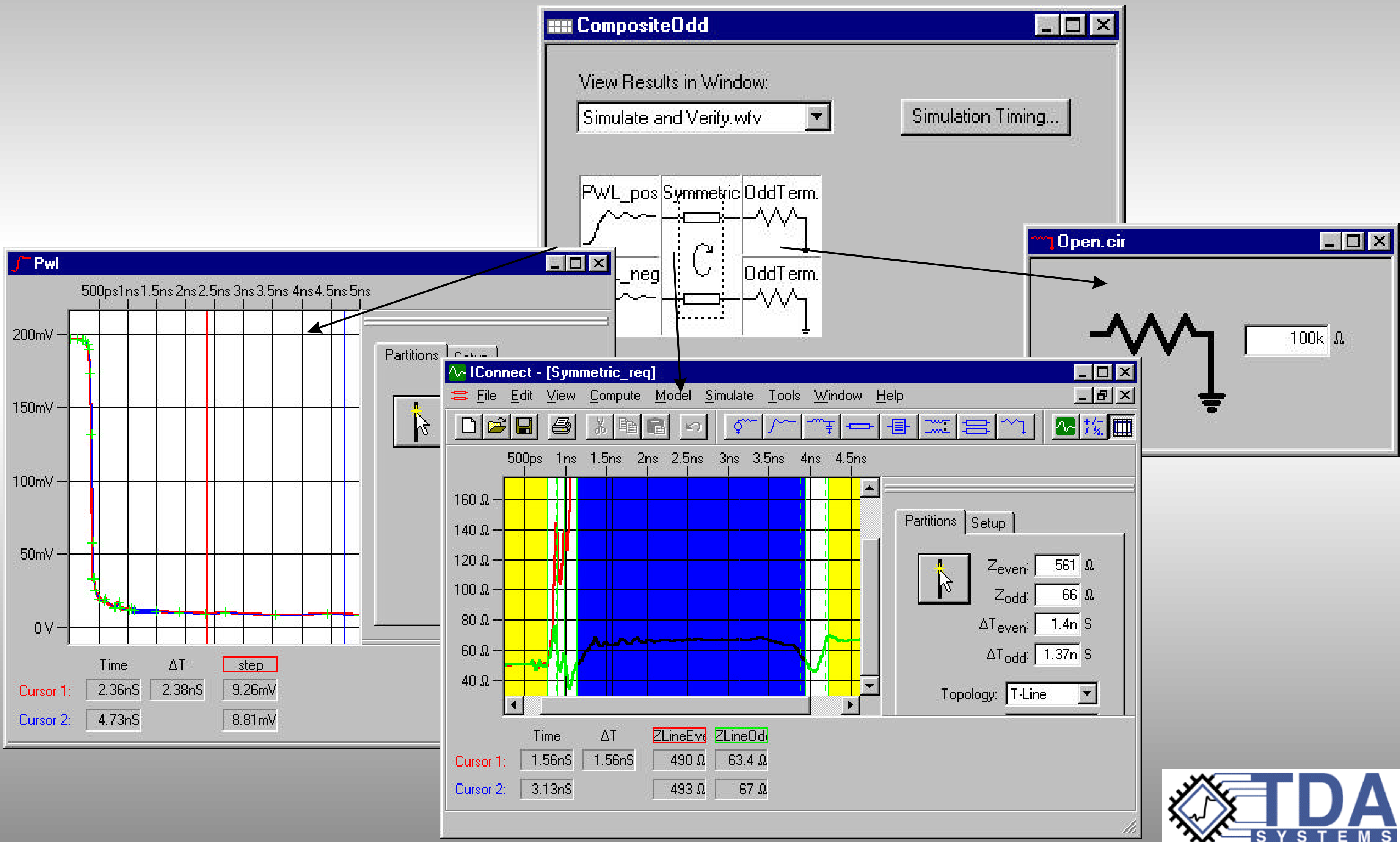
e5  28  26  28  29 2

e6  30  27  30  31 2

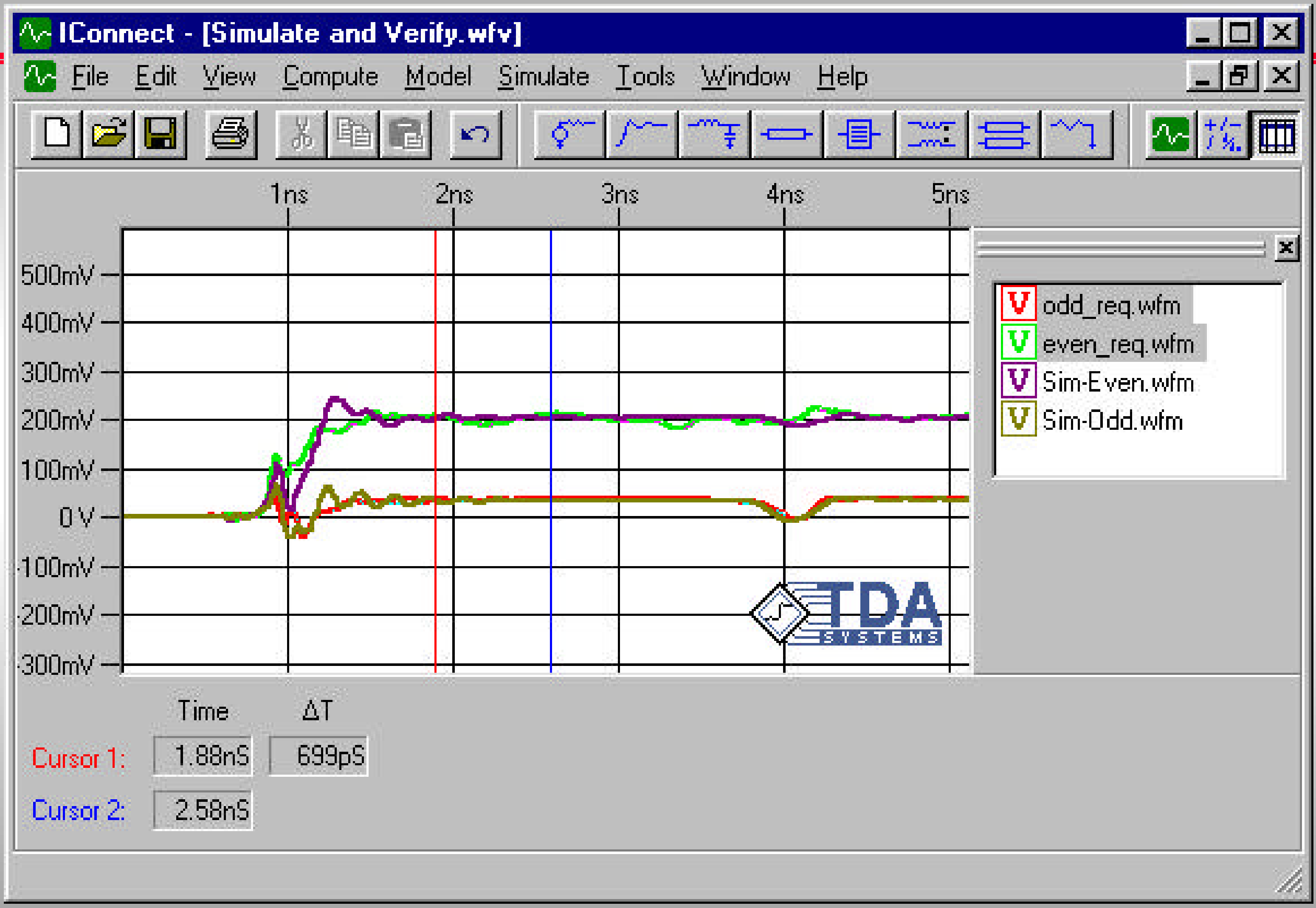
t11  28  29  30  31 Z0=22.9 TD=125p

t12  29  5  31  5 Z0=208 TD=140p

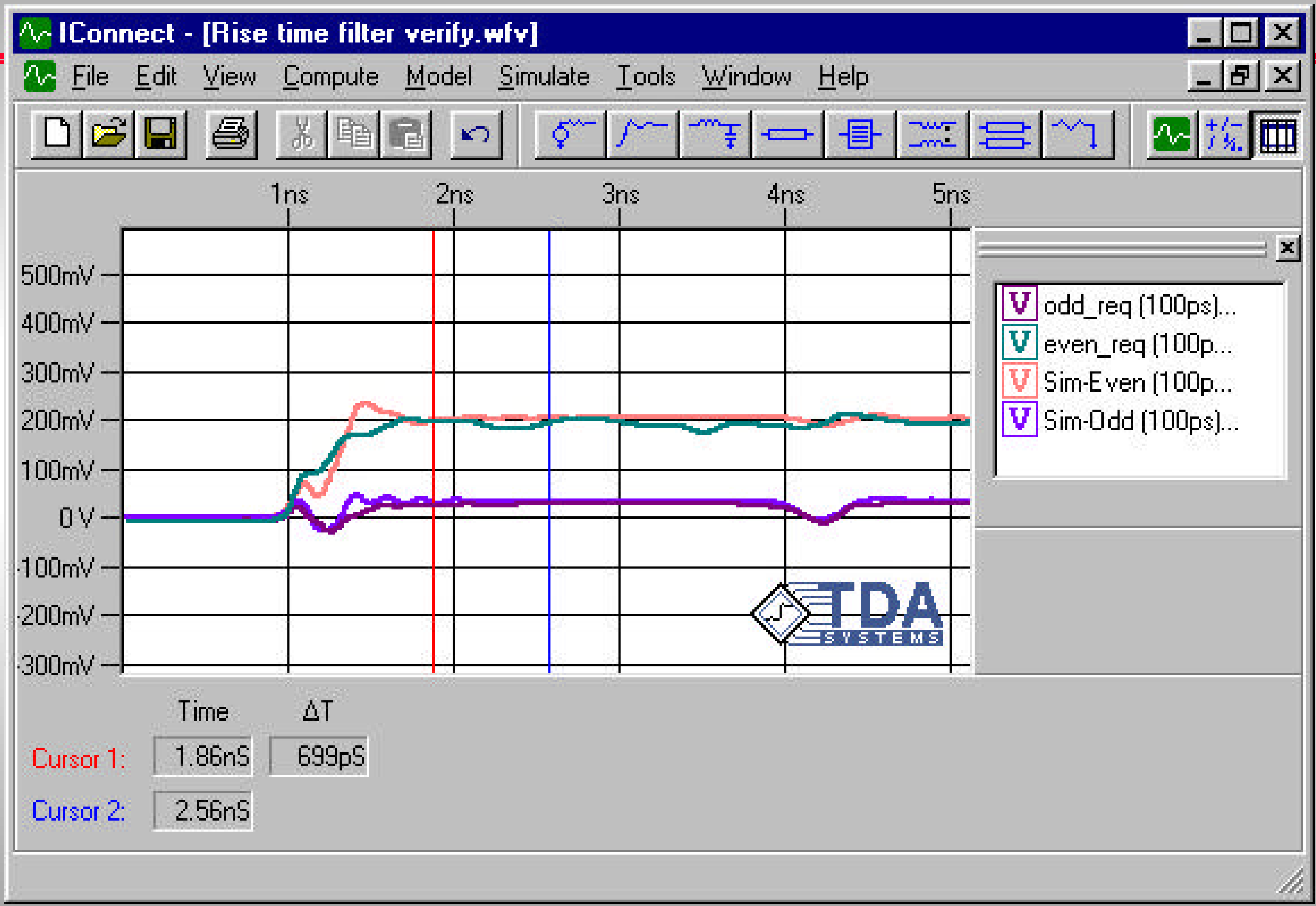
# Composite Model Generation



# Simulate and Verify

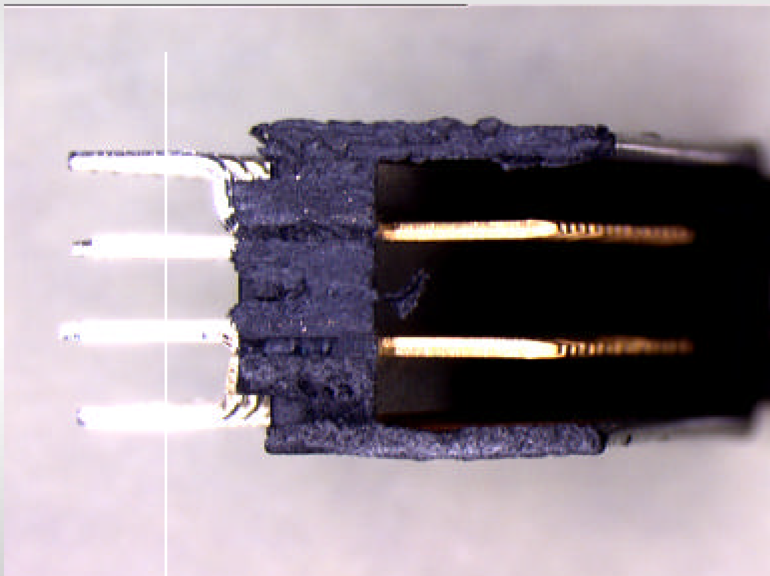


# Filter to Desired Rise Time

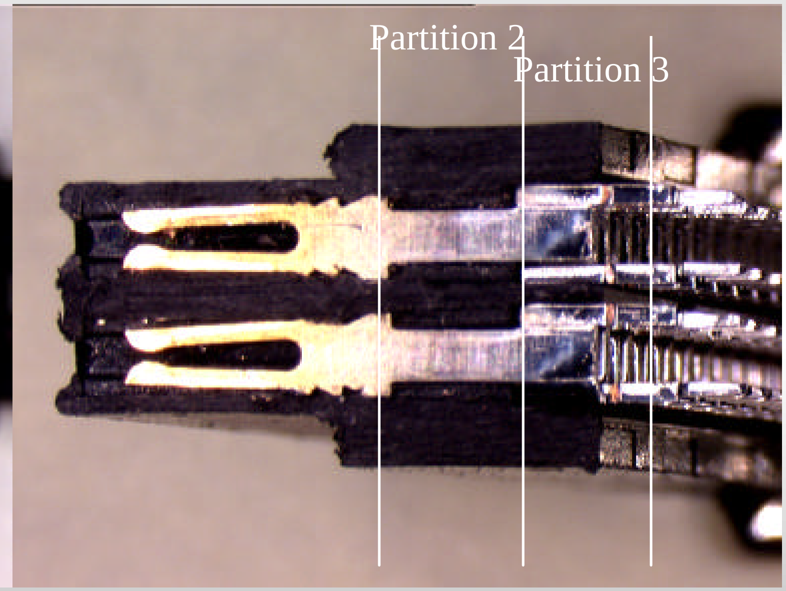


# Correlation to Physical Structure: Differential

PCB section



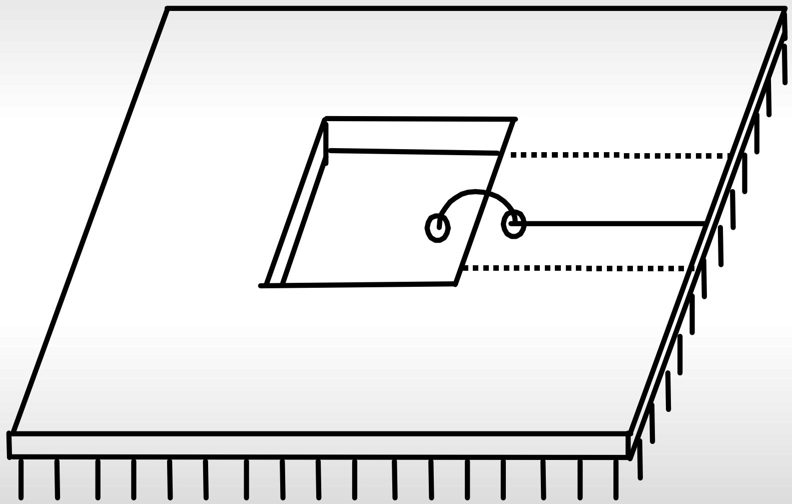
Cable section



# Summary and Further Work

- Accurate cable models are obtained
- Better understanding of connector geometries will improve the connector model

# Supplementary Information



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# Transmission line equation reference

$$Z_0 = \sqrt{\frac{R + jwL}{G + jwC}} \approx \sqrt{\frac{L}{C}}$$

$$V_p = \frac{1}{\sqrt{LC}}$$

$$L = Z_0 \cdot t_p \qquad C = \frac{t_p}{Z_0}$$

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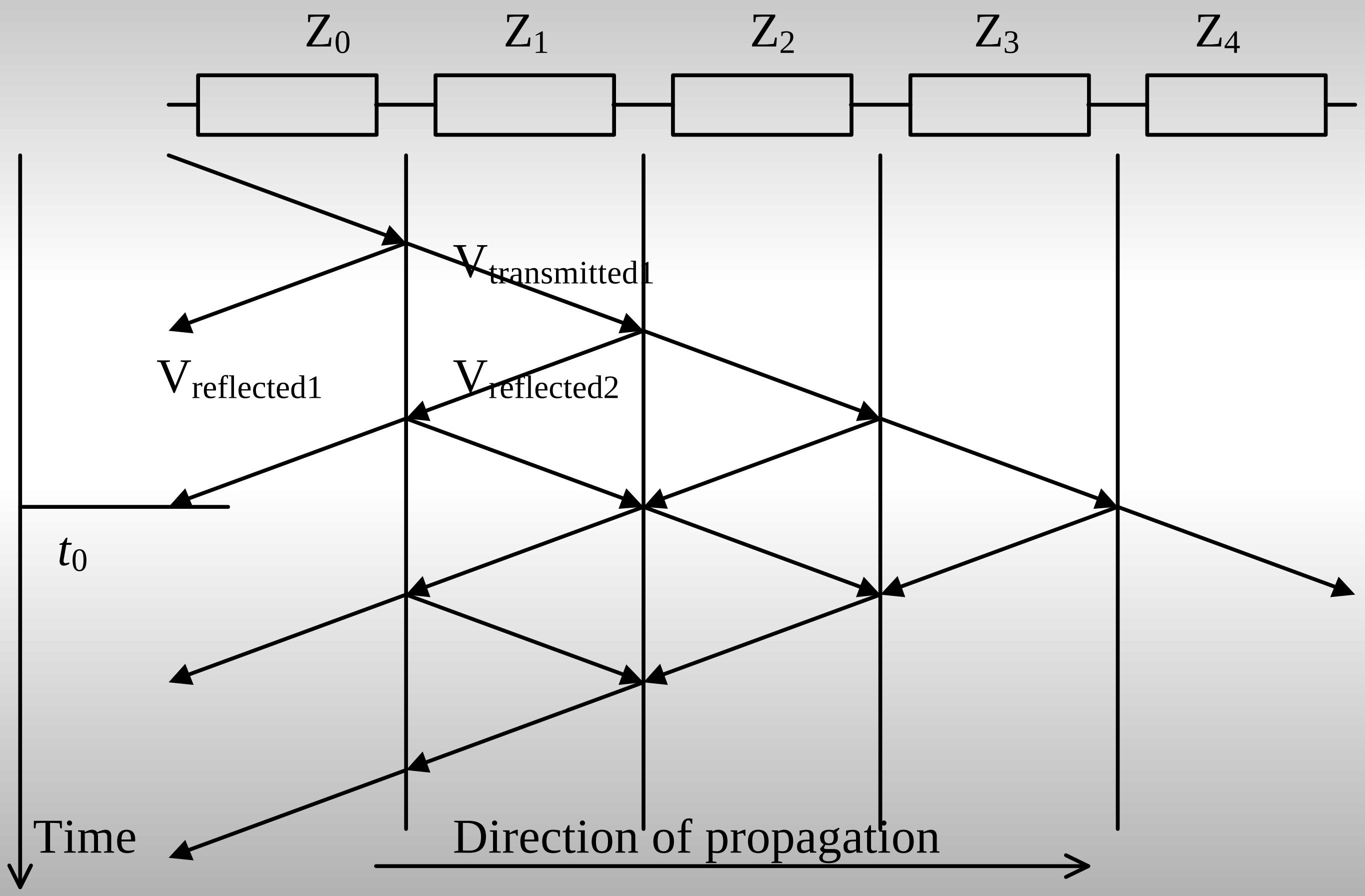
# Differential Transmission Line

$$Z_{even} = \sqrt{\frac{L_{self} + L_m}{C_{tot} - C_m}} \qquad Z_{odd} = \sqrt{\frac{L_{self} - L_m}{C_{tot} + C_m}}$$

$$t_{even} = \sqrt{(L_{self} + L_m)(C_{tot} - C_m)}$$

$$t_{odd} = \sqrt{(L_{self} - L_m)(C_{tot} + C_m)}$$

# TDR Multiple Reflection Effects

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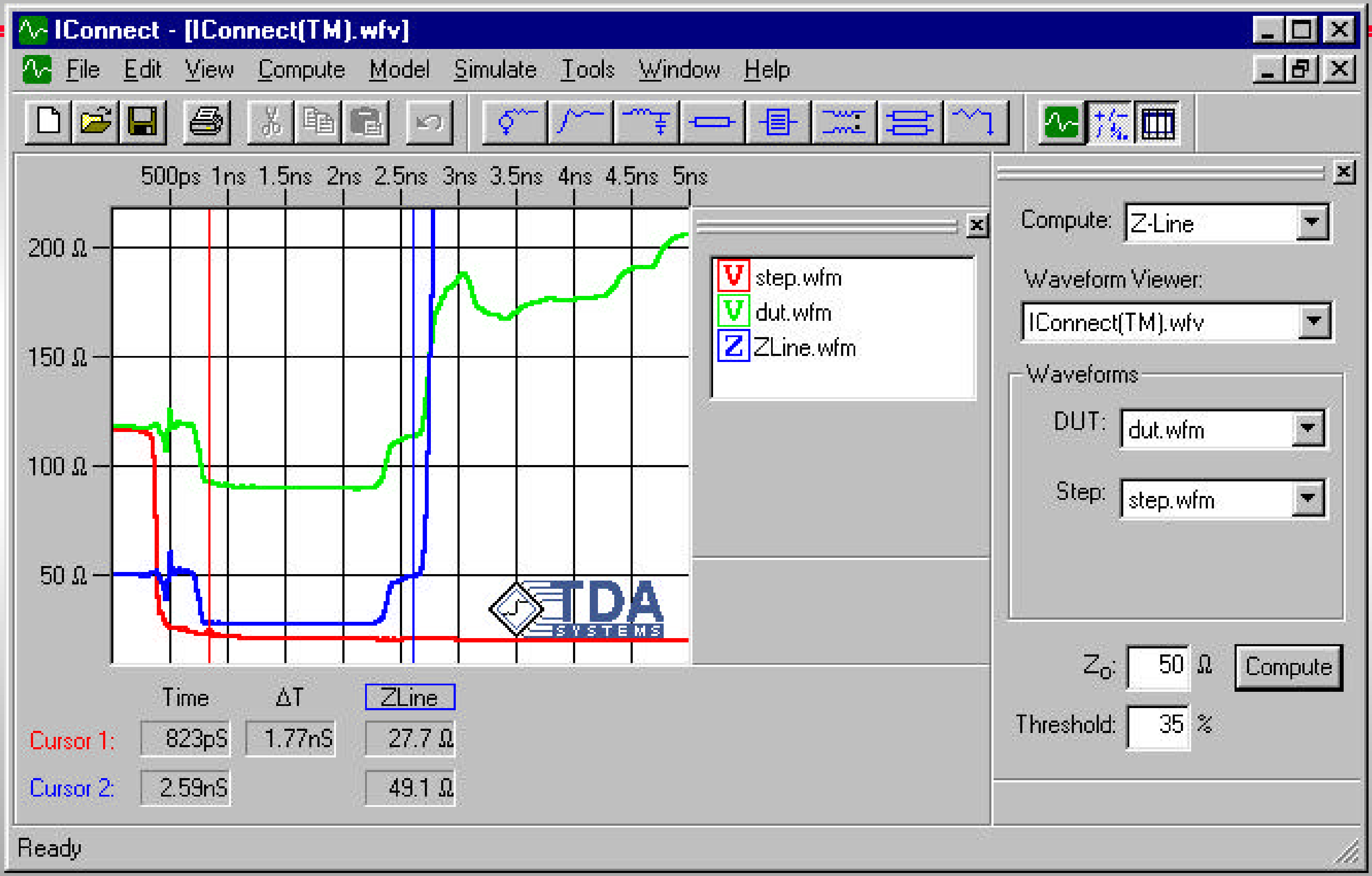
# Z-line Example

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# L-C Even-Odd Mode Analysis for Line with Constant Impedance

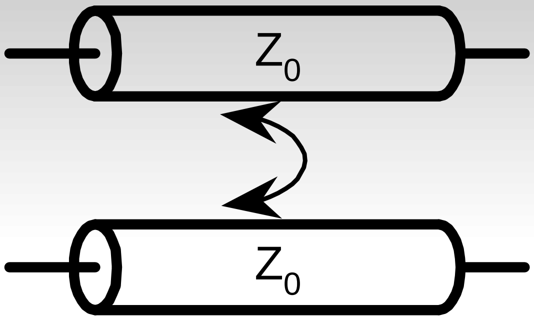
$$L = \frac{1}{2}\left(t_{even} Z_{even} + t_{odd} Z_{odd}\right)$$

$$C = \frac{t_{even}}{Z_{even}}$$

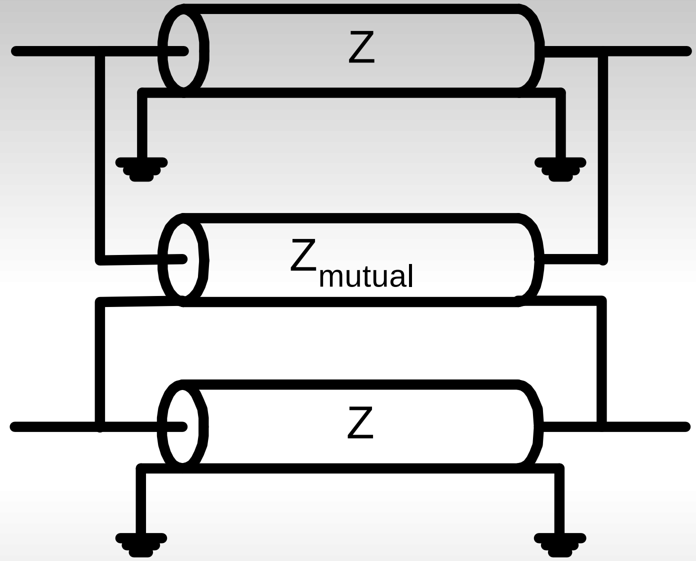
$$L_m = \frac{1}{2}\left(t_{even} Z_{even} - t_{odd} Z_{odd}\right)$$

$$C = \frac{1}{2}\left(\frac{t_{odd}}{Z_{odd}} - \frac{t_{even}}{Z_{even}}\right)$$

# 3-Line Symmetrical Coupled Line Model




$\Rightarrow$




$$Z = Z_{even}$$

$$Z_m = \frac{2Z_{odd}Z_{even}}{Z_{even} + Z_{odd}}$$

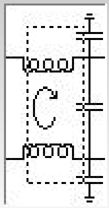
**Note:** $Z_0 = \sqrt{Z_{odd} Z_{even}}$

**! assume: $t_{odd}$=$t_{even}$ !**

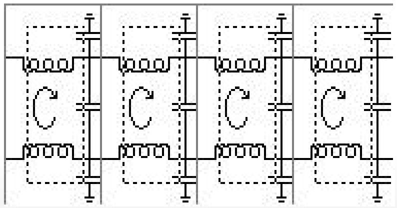
**Alternatively, for differential lines: $t_{mutual}$ = $t_{odd}$**

# Differential Line Modeling

- **Short interconnect**
  - **use lumped-coupled model**

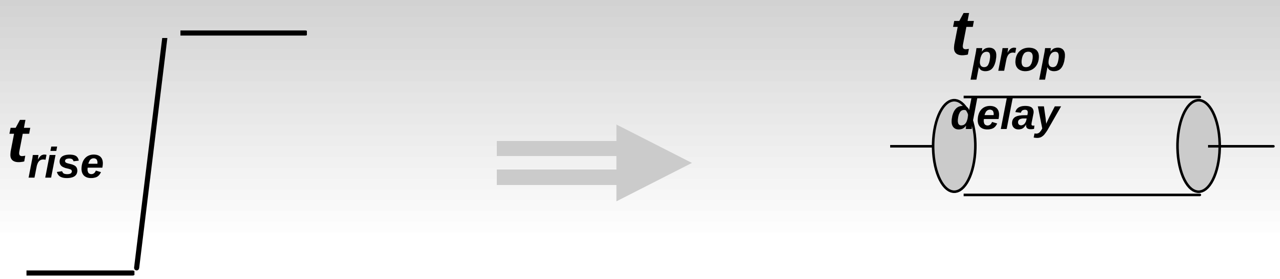



- **Long interconnect**
  - **split lines in multiple segments**




- **Longer yet interconnect**
  - **symmetric distributed coupled line model**

# Can you ignore interconnect effects?



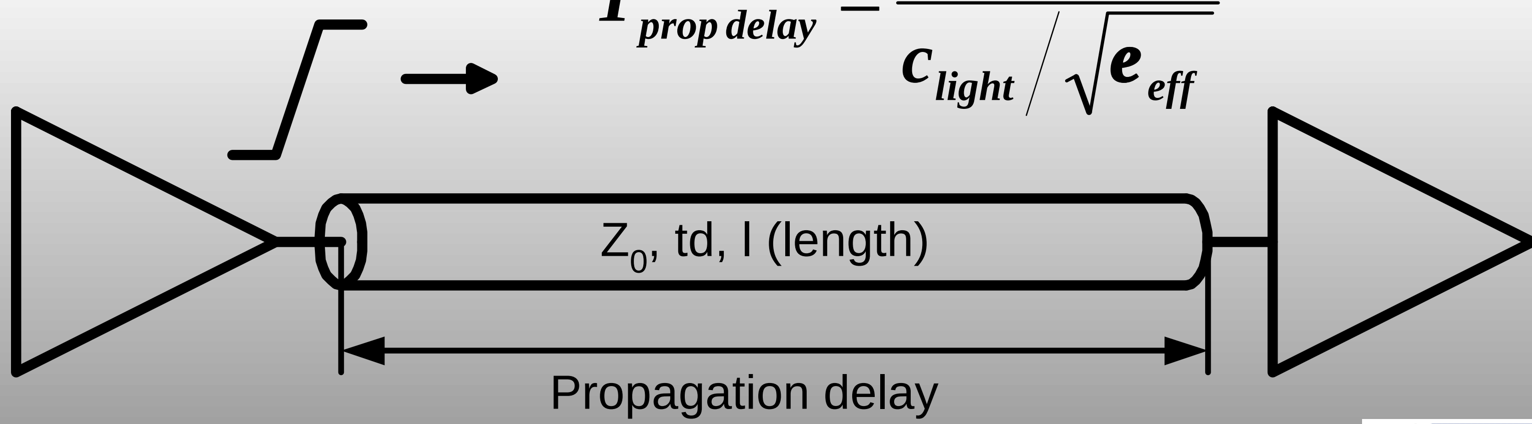

**Practical rule of “short” or “lumped” (RLC) interconnect**

$$t_{rise} > t_{prop\ delay} \bullet 6$$

# Propagation delay

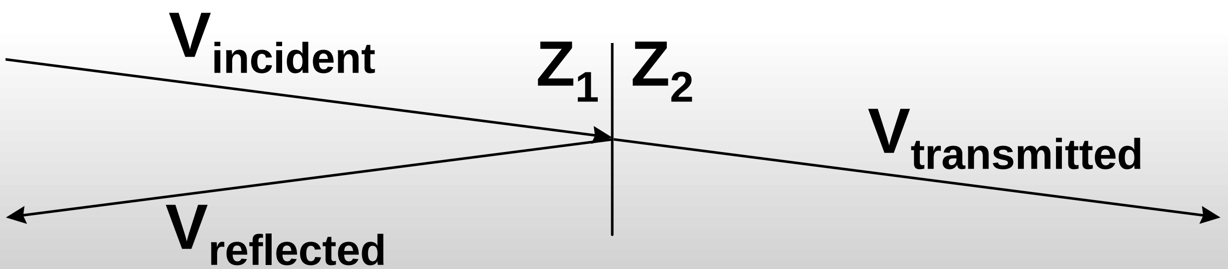
- Time required for signal to propagate through interconnect
- Dependent on velocity and interconnect length
- Examples:
  - prop. delay in vacuum: $1/c_{light}$=1 ns/foot (velocity $3 \cdot 10^8$ m/sec)
  - propagation delay per length in FR4: 150ps/inch

$$T_{prop\,delay} = \frac{l}{c_{light} / \sqrt{e_{eff}}}$$



# Reflections in Interconnects

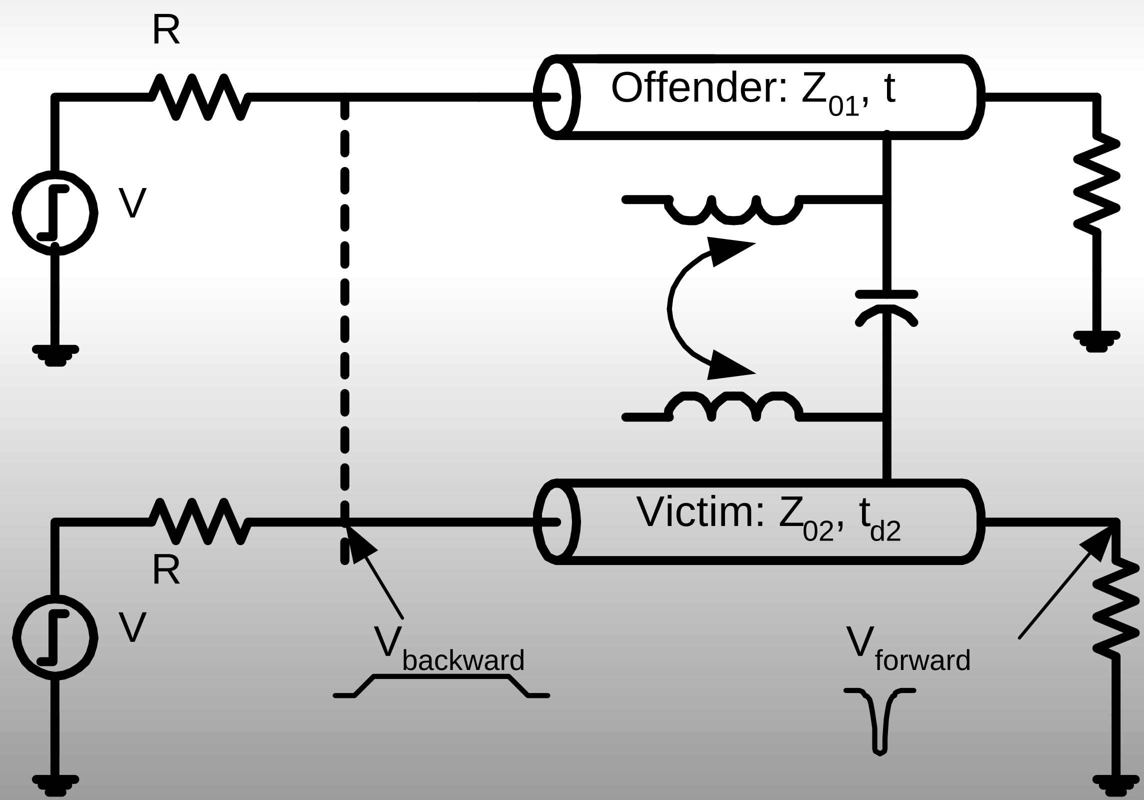
- Interconnects are transmission lines
- Impedance is the measure of *transmission properties* of interconnects
- In *any transmission media*, at the impedance discontinuity part of the energy is reflected back




**Reflection coefficient:** $$\Gamma = \frac{V_{reflected}}{V_{incident}} = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

# Crosstalk

- Energy coupling between adjacent lines
- Forward (far-end) and backward (near-end)
- Sum of capacitive and inductive



# Losses

- **Skin effect losses**

$$R_s = \frac{g}{P}\sqrt{\frac{p \cdot m}{s}} \cdot \sqrt{f} \quad \Omega/\text{inch}$$

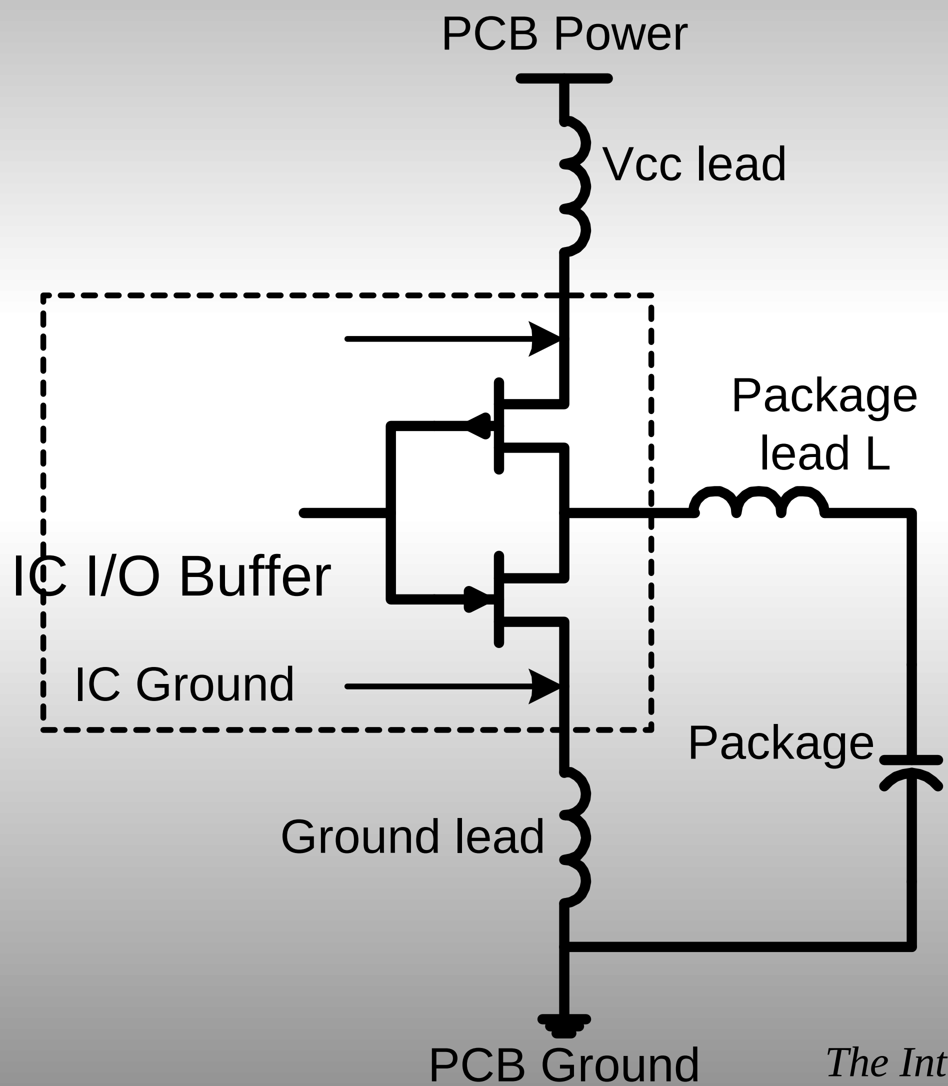
**Example (copper):**

$$R = \frac{g}{P} \cdot 3.07 \cdot 10^{-7} \cdot \sqrt{f} \quad \Omega/\text{inch}$$

- **Dielectric Losses**

$$G = g_d \cdot 2 \cdot p \cdot f \cdot e \cdot \tan d$$

# Ground Bounce, or Simultaneous Switching Noise (SSN)




- **SSN cause: inductance between IC, package and PCB ground**
- **SSN factors:**
  - **signal rise time**
  - **number of simultaneously switching buffers**
  - **package inductance**
  - **load capacitance**

# Rise time degradation

$$t_{\text{interconnect}} = \frac{0.35}{BW_{\text{interconnect}}}$$

$$t_{r\ final} = \sqrt{t_{signal}^{2} + t^{2}_{\text{interconnect}}}$$