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A Draft Proposal for Electrical Model Requirements of SCSI Interconnect Components

Revision 0

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1. References

1. SCSI Parallel Interface-3 (SPI-3) Working Draft American National Standard T10 Project 1302D Revision 10.
2. Guideline for Developing and Documenting Package Electrical Models Derived from Computational Analysis EIA/JEP126, JEDEC JC-15 Committee, May 1996.
3. Star-Hspice Manual Release 1999.2 June 1999, Avant! Corp

2. Scope

This guideline provides a methodology and specific requirements for creation, documentation and use of electrical models for SCSI passive interconnect components including connectors, cables, and printed circuits. The requirements outlined herein pertain to SCSI as defined by the SPI-3 Standard (see Reference 1).

3. Introduction

An interconnect electrical model is a circuit representation that approximates the electrical behavior of the interconnect component. These models may be generated by a variety of means including electromagnetic field analysis and circuit extraction from Time Domain Reflectometer (TDR) or Vector Network Analyzer (VNA) measurements. The resultant model is usually incorporated into a higher level simulation, such as SPICE, that can predict overall circuit performance.

Circuit simulations of SCSI interconnects typically require models at two levels of complexity: single-line and multi-line. Single-line models describe the transmission behavior of a single signal including its return path. Multi-line models describe the transmission behavior of several signals and return paths along with the mutual coupling that exists between all the individual signals by virtue of their proximity, conductor geometry and the physical properties of the respective materials (e.g. conductivity, permittivity, permeability, etc.). While manufacturing process variations may influence the electrical characteristics of any given population of interconnect components, this guideline will address only the nominal case model with typical values for all properties.

4. Model Requirements for Interconnect Components

4.1 Model inputs

4.1.1 Signal waveforms

The general parameters regarding signal amplitudes and timings of the stimulus waveforms shall be as described in the SPI-3 Standard (see Reference 1) unless otherwise specified.

4.1.2 Frequency range

While the spectral content of a SCSI signal depends heavily on the rise time of driver circuit and may contain measurable frequency components into the microwave region, for SPI-3 SCSI simulation purposes the frequency range of primary interest may be assumed as zero to six hundred megahertz inclusive, unless otherwise specified.

4.1.3 Rise time

Signal rise time describes the time interval required for a signal to rise or fall between two specified limits. Model developers and model users alike should be aware that the rise times listed in various specifications (including SPI-3) may define threshold limits that differ from those used by simulation tools and that some interpolation or extrapolation may be required to derive values with consistent threshold limits. For example, simulators frequently define rise time as the interval between the 0% and 100% points of the steady state response, whereas SPI-3 defines rise times between the 20% and 80% points. For the purposes of SPI-3 SCSI simulation the rise times may be assumed as listed below unless otherwise specified.

- Interconnects for Single-Ended (SE) SCSI : rise time (0-100%) = 3.0 nS minimum
- Interconnects for Low Voltage Differential (LVD) SCSI: rise time (0-100%) = 1.0 nS minimum

4.2 Model Complexity

Single-line models shall describe a single signal path which includes both outgoing and return current paths.

Multi-line models shall describe a primary signal path (with source and return current conductors) along with the six closest adjacent secondary signal paths (which also include source and return current conductors). For example, a model for multiconductor flat ribbon cable would include a primary conductor pair along with the three adjacent pair on either side of the primary pair for a total of seven conductor pairs (14 wires). (*Ed note: issues here, final wording TBD*)

Interconnect components which exhibit significant variation between conductor pairs (such as central pairs versus exterior pairs in a cable) shall provide separate models for each extreme condition.

Interconnect components with insulators which exhibit significant variations in permittivity or dielectric loss over the frequency range specified above shall provide separate models for each relative maxima and minima and shall specify the range of frequencies where each model is valid. (*Ed note: issues here, final wording TBD*)

4.3 Model formats

Interconnect models can be presented in a variety of ways depending on the methods used to derive the model parameters. For SPI-3 SCSI simulation under this guideline, models shall be provided in at least one of the formats listed below. All model parameters shall be specified in terms of fundamental MKS units (i.e. ohms, henrys, mhos, farads, meters and seconds).

4.3.1 Mixed lumped element and transmission line equivalent circuit format

This model format consists of a SPICE subcircuit composed of lumped R, L and C elements along with T, U, and W transmission line elements and K coupling elements. The single-line model node definition is shown in Figure 1 below. The multi-line model node definition is shown in Figure 2 below. For consistency, multi-line model nodes seven and eight shall be considered the "driven" pair while nodes one through six and nine through fourteen are considered the "adjacent" pairs. Note that the subcircuit node numbers pictured here are not necessarily the same as the node numbers of any elements internal to the subcircuit.

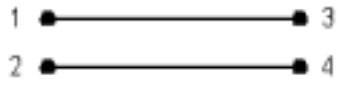
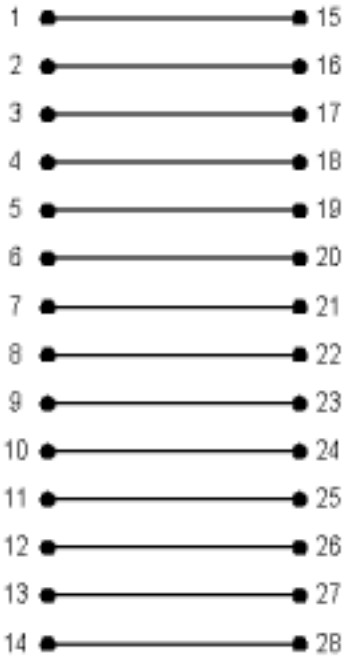


Figure 1. Single-line model subcircuit nodes



(Ed note: renumber nodes 1A-1B, etc)

Figure 2. Multi-line model subcircuit nodes

4.3.2 RLGC matrix format

Maxwellian or branch-circuit representation. Details tbd.

4.4 Model validation

Each model shall be validated to ensure its accuracy. Methods & criteria TBD. *(Ed note: see examples at IBIS web page.)*

4.5 Model documentation

Each model shall include the information listed below. In addition, models may include copyright and/or confidentiality statements as necessary.

1. Model equivalent circuit description formatted as specified above.
2. Model version status and brief revision history.
3. Model limitations and/or dependencies (if any).
4. Special instructions (if any) regarding use of the model or interpretation of the results.
5. Model derivation method(s): how was the model created (electromagnetic field analysis, extraction by TDR methods, etc.). List specific commercial apparatus or software package name and version where appropriate.
6. Model validation: how was the model verified. List specific measurements and/or simulation cases and summarize results. Measurement and simulation data may be included for comparison. Address discrepancies where necessary.
7. Model support contact information.

The model equivalent circuit description shall be contained in one or more ASCII text (.txt) files. All other textual documentation shall be contained in one or more ASCII text (.txt) or Portable Document Format (.pdf) files. Graphical information (such as measurement and simulation results) may be contained in one or more Windows Bitmap (.bmp), Tagged Image Format (.tif), or Joint Photographics Experts Group (.jpg) files. If the model contains more than one file, then the model shall also include a file named "README.txt" which contains a list of all the other file names that belong to the model along with a brief description of the contents of each file. Complete model packages shall have all files grouped and compressed into a single file in both PC archive (.zip) and Unix archive (.tar) file formats. (See t10.org for details regarding generation of .zip and .tar files.)

4.6 Model Availability

Simulation models must be made available in a timely manner to control risk and facilitate useful system design validation. While specific availability requirements are beyond the scope of this guideline, manufacturers of SCSI interconnect components are encouraged to make model development an integral part of their product design process and to support model availability from product announcement through end of production.