SCSI signal modeling study group (SSM)   00-111r0
December 01, 1999
Rochester, MN, CA
Subject: Draft minutes for the SSM working group on December 01, 1999

This was the next meeting to address the general subject of modeling for
parallel SCSI. Jonathan Fasig of Western Digital led the meeting in the
absence of Dean Wallace. Bill Ham of Compaq took these minutes. There
was a good attendance from a broad spectrum of the industry. Western
Digital (Jonathan Fasig) hosted the meeting.

Last approved minutes: 99-329r1.

1. AGENDA SSM MEETING (ROCHESTER MN)

2. Introductions

Jonathan Fasig, substituting for Dean Wallace, opened the meeting and
conducted the introductions and reviewed the meeting purpose. Bill Ham
thanked Jonathan for hosting the meeting.

3. Attendance

The following folks were present:

Martin Ogbuokiri, Molex, mogbuokiri@molex.com
Larry Barnes, LSI Logic, larry.barnes@lsil.com
Jonathan Fasig, Western Digital, jonathan.L.Fasig@wdc.com
Tariq Abou-Jeyab, Adaptec, tajeyab@corp.adaptec.com
Bill Ham, Compaq, bill_ham@ix.netcom.com
Andrew Bishop, Quantum, andrew.bishop@quantum.com
Dave Chapman, Amphenol, dave.chapman@aipc.fabrik.com
Greg Vaupotic, Amphenol, gerg.vaupotic@snet.net
Paul Aloisi, TI, Paul_Alosis@ti.com
Nicholaos Limberopoulos, C&M, Nlimberopoulos@cm-corp.com
Thom Kreusel, HP, Thom_Kreusel@HP.com
Dan Smith, Seagate, daniel_f_smith@notes.seagate.com
Greg Doyle, Mentor Graphics, greg-doyle@mentor.com
Larry Stanley, Mentor Graphics, larry_stanley@mentor.com
Dima Smolyansky, TDA systems, dima@tdasystems.com
Rollie O'Groske, JPM, Jit2pan3@us.ibm.com
Jeff Rosa, Amphenol Interconnect, Jeff.rosa@aipc.fabrik.com

4. Agenda development

The agenda shown was that used.

5. Call for vice chair

It being recognized that Dean is not always available and that further
administrative energy may be needed from time to time a call was made
for folks interested in being vice chair of the SSM working group. This
call will remain open until the next meeting at which time a permanent
appointment will be made.

At this meeting only Jonathan Fasig indicated an interest. This subject
will be readdressed at the next meeting but Jonathan will be acting as
vice chair for this meeting.

6. Approval of previous minutes

The minutes of the last meeting were reviewed and minor changes were
made. Bill Ham moved and Tariq seconded that these revised minutes be
approved. Motion passed unanimously.

7. Action item review

The action items were reviewed with the status indicated in the action
item section of the minutes.

8. Presentation Policy

This item is included for easy reference and will be retained in future
minutes.

It is the policy of the SSM working group that all material presented at
the SSM working group shall be made available electronically and posted
on the T10 web site.

Material presented at the meeting should be uploaded to the T10 web site
two weeks prior to the meeting. Alternatively the material may be
electronically supplied to the chair or secretary at the meeting where
the material is presented at the discretion of the chair.

Material should be free from any statement of confidentiality or
restriction of use and should not contain any pricing or product
scheduling information.

9. SSM project proposal - Ham

The SSM project was approved at the last T10 plenary. A project number
will be available shortly.

10. Presentations

10.1 IBIS status (Larry Barnes) (10 min)

Larry gave the following presentation relating to an attempt to include
the ISI and multilevel signals into IBIS:
```
===========================================================================
|     Keyword:  [Driver Schedule]
|    Required:  No
| Description:  Describes the relative model switching sequence for referenced
|               models to produce a multi-staged driver.
| Usage Rules:  The [Driver schedule] keyword establishes a hierarchical order
|               between models and should be placed under the [Model] which
|               acts as the top-level model.  The scheduled models are then
```

referenced from the top-level model by the [Driver Schedule] keyword.

When a multi-staged buffer is modeled using the [Driver Schedule] keyword, all of its stages (including the first stage, or normal driver) have to be modeled as scheduled models.

If there is support for this feature in a simulator, the [Driver Schedule] keyword will cause it to use the [Pulldown], [Pulldown Reference], [Pullup], [Pullup Reference], [Voltage Range], [Ramp], [Rising Waveform] and [Falling Waveform] keywords from the scheduled models instead of the top-level model, according to the timing relationships described in the [Driver Schedule] keyword. Consequently, the keywords in the above list will be ignored in the top-level model. Also, all other keywords not shown in the above list will be ignored in the scheduled model(s).

However, both the top-level and the scheduled model(s) have to be complete models, i.e. all of the required keywords must be present and follow the syntactical rules.

For backwards compatibility reasons and for simulators which do not support multi-staged switching, the keywords in the above list can be used in the top-level [Model] to describe the overall characteristics of the buffer as if it was a composite model. It is not guaranteed, however, that such a top-level model will yield the same simulation results as a full multi-stage model. It is recommended that a "golden waveform" for the device consisting of a [Rising Waveform] table and a [Falling Waveform] table be supplied in the top-level model to serve as a reference for validation.

Even though some of the keywords are ignored in the scheduled model, it may still make sense in some cases to supply correct data with them. One such situation would arise when a [Model] is used both as a regular top-level model as well as a scheduled model.

The [Driver Schedule] table consists of five columns. The first column contains the model names of other models that exists in the .ibs file. The remaining four columns describe delays: Rise_on_dly, Rise_off_dly, Fall_on_dly, and Fall_off_dly. The t=0 time of each delay is the event when the simulator's internal pulse initiates a rising or falling transition. All specified delay values must be equal to or greater than 0. There are only five valid combinations in which these delay values can be defined:

```
    1)  Rise_on_dly     with    Fall_on_dly
    2)  Rise_off_dly    with    Fall_off_dly
    3)  Rise_on_dly     with    Rise_off_dly
    4)  Fall_on_dly     with    Fall_off_dly
    5)  All four delays defined
        (be careful about correct sequencing)
```

The four delay parameters have the meaning as described below. (Note that this description applies to buffer types which have both pullup and pulldown structures. For those buffer types which have only a pullup or pulldown structure, the description for the missing structure can be omitted.)

Rise_on_dly is the amount of time that elapses from the internal simulator pulse initiating a RISING edge to the t=0 time of the waveform or ramp that turns the I-V table of the PULLUP device ON, and the t=0 time of the waveform or ramp that turns the I-V table of the PULLDOWN device OFF (if they were not already turned ON and OFF, respectively, by another event).

Rise_off_dly is the amount of time that elapses from the internal simulator pulse initiating a RISING edge to the t=0 time of the waveform or ramp that turns the I-V table of the PULLUP device OFF, and the t=0 time of the waveform or

| ramp that turns the I-V table of the PULLDOWN device ON (if
| they were not already turned ON and OFF, respectively, by
| another event).
|
| Fall_on_dly is the amount of time that elapses from the
| internal simulator pulse initiating a FALLING edge to the
| t=0 time of the waveform or ramp that turns the I-V table of
| the PULLDOWN device ON, and the t=0 time of the waveform or
| ramp that turns the I-V table of the PULLUP device OFF (if
| they were not already turned ON and OFF, respectively, by
| another event).
|
| Fall_off_dly is the amount of time that elapses from the
| internal simulator pulse initiating a FALLING edge to the
| t=0 time of the waveform or ramp that turns the I-V table of
| the PULLDOWN device OFF, and the t=0 time of the waveform or
| ramp that turns the I-V table of the PULLUP device ON (if
| they were not already turned ON and OFF, respectively, by
| another event).
|
| Note that some timing combinations may only be possible if
| the two halves of a complementary buffer are modeled
| separately as two open_* models.
|
| Use 'NA' when no delay value is applicable. For each
| scheduled model the transition sequence must be complete,
| i.e., the scheduled model must return to its initial state.
|
| No [Driver Schedule] table may reference a model which
| itself has within it a [Driver Schedule] keyword.
|
| Other Notes: The added models typically consist of Open_sink (Open_drain)
| or Open_source models to provide sequentially increased drive
| strengths. The added drive may be removed within the same
| transition for a momentary boost or during the opposite
| transition.
|
| The syntax also allows for reducing the drive strength.
|
| Note that the Rise_on_dly, Rise_off_dly, Fall_on_dly,
| Fall_off_dly parameters are single value parameters, so
| typical, minimum and maximum conditions cannot be described
| with them directly. In order to account for those effects,
| one can refer to the fastest waveform table with the delay
| number and then insert an appropriate amount of horizontal
| lead in section in those waveforms which need more delay.
|
| Notice that the C_comp parameter of a multi-stage buffer is
| defined in the top-level model. The value of C_comp
| therefore includes the total capacitance of the entire
| buffer, including all of its stages. Since the rising and
| falling waveform measurements include the effects of
| C_comp, each of these waveforms must be generated with the
| total C_comp present, even if the various stages of the
| buffer are characterized individually.
|
| Note: In a future release, the [Driver Schedule] keyword may
| be replaced by a newer method of specification that is
| consistent with some other planned extensions. However, the
| [Driver Schedule] syntax will continue to be supported.
|--
[Driver Schedule]
| Model_name   Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly
  MODEL_OUT   0.0ns   NA   0.0ns   NA
|
| Examples of added multi-staged transitions
  M_O_SOURCE1   0.5ns   NA   0.5ns   NA
| low (high-Z) to high   high to low (high-Z)
  M_O_SOURCE2   0.5n   1.5n   NA   NA
| low to high to low   low (high-Z)
  M_O_DRAIN1   1.0n   NA   1.5n   NA
| low to high (high-Z)   high (high-Z) to low
  M_O_DRAIN2   NA   NA   1.5n   2.0n
| high (high-Z)   high to low to high

|

Larry noted that it may require inclusion of certain logic paths that
define the signals for ISI compensation in the modeling methodology.
This will be a new capability for any present tool since it for

10.2 Network parameters annex proposal (Larry Barnes) (10 min)

Larry offered the following material that explains the situation with
network paramaters. This material will become an informative annex in
the document.

10.2.1 Networks

10.2.1.1 N-port networks

N-port networks relate the voltages and currents at various points in a
transmission network through the use of impedance or admittance matrices of
circuit theory. They describe a matrix equivalent of the network.   A port is
the term used to replace the more cumbersome phrase "two-terminal pair".
The ports in Figure 10-1 may be any transmission line or equivalent
propagating a single mode. Multiple propagation modes need not be
considered in the SCSI environment, since multiple propagation modes are
only supported in waveguides. A terminal plane, t_n, is defined along with the
incident and reflected wave's equivalent voltages and currents. At the nth
terminal plane the total voltage and current is given by

$$V_n = V_n^+ + V_n^-$$

$$I_n = I_n^+ + I_n^-$$

Equation 10-1 N-port voltage and current

when $z=0$.

These voltages and currents are then related through an impedance [Z] matrix,
Equation 10-2, and admittance [Y] matrix, **Error! Not a valid bookmark
self-reference.**, for the N-port network.

$$
\begin{bmatrix} V_1 \\ V_2 \\ \\ \vdots \\ V_N \end{bmatrix}
=
\begin{bmatrix}
Z_{11} & Z_{12} & Z_{13} & \cdots & Z_{1N} \\
Z_{21} & Z_{22} & \cdots & \cdots & Z_{2N} \\
Z_{31} & \vdots & & & \vdots \\
\vdots & \vdots & \vdots & & \vdots \\
Z_{N1} & Z_{N2} & \cdots & \cdots & Z_{NN}
\end{bmatrix}
\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ \vdots \\ I_N \end{bmatrix}
$$

Equation 10-2   N-port impedance matrix

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & \cdots & Y_{1N} \\ Y_{21} & Y_{22} & \cdots & \cdots & Y_{2N} \\ Y_{31} & \vdots & & & \vdots \\ \vdots & \vdots & \vdots & & \vdots \\ Y_{N1} & Y_{N2} & \cdots & \cdots & Y_{NN} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ \vdots \\ V_N \end{bmatrix}$$

Equation 10-3   N-port admittance matrix

In general the impedance and admittance matrices are symmetric. For example,

$$Z_{ij} = Z_{ji}$$

Figure 10-1   Arbitrary N-port network

In general it is difficult to define voltages and currents for non-TEM modes of propagation. Fortunately SCSI interconnects presently only support TEM and quasi-TEM modes of propogation. A practical problem exists when trying to measure voltages and currents at high frequencies because of the relationships between magnitude and phase of the signal. The scattering matrix [S] solves this problem. The scattering parameters relate the incident and reflected voltage waves at the ports, Equation 10-4, and does not necessariy need be symmetric. They can be directly obtained with a vector network analyzer. Other N-port matrix parameters are easily obtained through conversion.

$$\begin{bmatrix} V_1^- \\ V_2^- \\ V_3^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \cdots & S_{1N} \\ S_{21} & S_{22} & \cdots & \cdots & S_{2N} \\ S_{31} & \vdots & & & \vdots \\ \vdots & \vdots & \vdots & & \vdots \\ S_{N1} & S_{N2} & \cdots & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ V_3^+ \\ \vdots \\ V_N^+ \end{bmatrix}$$

Equation 10-4   N-port scattering matrix

An n-port network can be characterized by Y, Z, and S parameters, but in general most networks consist of a cascade of two-port networks. The one main exception is the place a stub attaches to the bus.

10.2.1.1.1 Conversion between two-port network parameters

	S	**Z**	**Y**	**ABCD**
S_{11}	S_{11}	$\dfrac{(Z_{11}-Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}{\Delta Z}$	$\dfrac{(Y_0-Y_{11})(Y_0+Y_{11})+Y_{12}Y_{21}}{\Delta Y}$	$\dfrac{A+B/Z_0-CZ_0-D}{A+B/Z_0+CZ_0+D}$
S_{12}	S_{12}	$\dfrac{2Z_{12}Z_0}{\Delta Z}$	$\dfrac{-2Y_{12}Y_0}{\Delta Y}$	$\dfrac{2(AD-BC)}{A+B/Z_0+CZ_0+D}$
S_{21}	S_{21}	$\dfrac{2Z_{21}Z_0}{\Delta Z}$	$\dfrac{-2Y_{12}Y_0}{\Delta Y}$	$\dfrac{2}{A+B/Z_0+CZ_0+D}$
S_{22}	S_{22}	$\dfrac{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}}{\Delta Z}$	$\dfrac{(Y_0+Y_{11})(Y_0-Y_{22})+Y_{12}Y_{21}}{\Delta Y}$	$\dfrac{-A+B/Z_0-CZ_0+D}{A+B/Z_0+CZ_0+D}$
Z_{11}	$Z_0\dfrac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{11}	$\dfrac{Y_{22}}{\lvert Y\rvert}$	$\dfrac{A}{C}$
Z_{12}	$Z_0\dfrac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{12}	$\dfrac{-Y_{12}}{\lvert Y\rvert}$	$\dfrac{AD-BC}{C}$
Z_{21}	$Z_0\dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{21}	$\dfrac{-Y_{21}}{\lvert Y\rvert}$	$\dfrac{1}{C}$
Z_{22}	$Z_0\dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{22}	$\dfrac{Y_{11}}{\lvert Y\rvert}$	$\dfrac{D}{C}$
Y_{11}	$Y_0\dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\dfrac{Z_{22}}{\lvert Z\rvert}$	Y_{11}	$\dfrac{D}{B}$
Y_{12}	$Z_0\dfrac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	$\dfrac{-Z_{12}}{\lvert Z\rvert}$	Y_{12}	$\dfrac{BC-AD}{B}$
Y_{21}	$Z_0\dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	$\dfrac{-Z_{21}}{\lvert Z\rvert}$	Y_{21}	$\dfrac{-1}{B}$
Y_{22}	$Z_0\dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	$\dfrac{Z_{11}}{\lvert Z\rvert}$	Y_{22}	$\dfrac{A}{B}$
A	$\dfrac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}}$	$\dfrac{Z_{11}}{Z_{21}}$	$\dfrac{-Y_{22}}{Y_{21}}$	A
B	$Z_0\dfrac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}}$	$\dfrac{\lvert Z\rvert}{Z_{21}}$	$\dfrac{-1}{Y_{21}}$	B
C	$\dfrac{1}{Z_0}\dfrac{(1-S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}}$	$\dfrac{1}{Z_{21}}$	$\dfrac{-\lvert Y\rvert}{Y_{21}}$	C
D	$\dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}}$	$\dfrac{Z_{22}}{Z_{21}}$	$\dfrac{-Y_{11}}{Y_{21}}$	D

$$\lvert Z\rvert = Z_{11}Z_{22}-Z_{12}Z_{21} \qquad\qquad \lvert Y\rvert = Y_{11}Y_{22}-Y_{12}Y_{21}$$

$$\Delta Z = (Z_{11}+Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21} \qquad \Delta Y = (Y_{11}+Y_0)(Y_{22}+Y_0)-Y_{12}Y_{21}$$

$$Y_0 = 1/Z_0$$

10.3 Methodology for extracting model parameters from TDR data (Dima Smolyansky - TDA systems) (1 hour)

A major presentation by TDA described a methodology for extracting RLGC parameters from actual passive SCSI interconnect assemblies. This presentation is available on the T10 web site as it is too large to fit in these minutes.

10.4 Tool Presentation (Mentor Graphics) (1 hour)

This presentation described some tools available from Mentor Graphics. This presentation will be available on the T10 web site as it is too large to fit in these minutes.

10.5 Modeled cable parameters (Greg Vaupotic) (10 min)

Greg presented a set of data where used a physical description of a cable media with inputs consisting of geometry, dielectric constant, loss tangent, and metals conductivity with the Ansoft Maxwell EX2D (inexpensive) field solver packages. He extracted inductance, capacitance, resistance, conductance (dielectric) parameters (as a function of frequency) to produce a simulated attenuation result that closely matched the experimental results.

This stands in contrast to a simpler modeling technique where the dielectric loss (conductance) and inductance were represented as square root of frequency dependencies.

The excellent agreement between the modeling results and the first principles simulation was better than expected. This result shows that it may be possible to get reliable results from interconnect simulations even for fairly sophisticated behavior.

10.6 Draft of proposal for modeling passive interconnects (Jonathan Fasig) (30 min)

In satisfaction of an action item from the last meeting Jonathan produced a document containing a proposal for a set of requirements on models. These requirements will be placed in the document in a section to be determined.

This work places requirements on the form and content of models so that they can be more easily used with different tools.

The text of this proposal is available on the T10 web site.

11. Matrix development for SSM

The following summarizes the present position for the SSM matrix. This
matrix is a concise description of the methodology to be used for the
respective areas of the point to point SCSI bus segment. Several of the
areas were significantly modified at this meeting. Note that the
multidrop areas have not yet been identified.

This section contains some repeated information from the last minutes as
it continues to be relevant and current.

11.1 Transceiver chips: owner, Dean Wallace

No new content info this meeting.

Interface is at packaging pins
Model types: Spice, IBIS, HDL, table spice – details TBD
Data patterns: TBD
ISI compensation: required but not presently believed compatible with
IBIS capability – this means that IBIS will have to be enhanced and that
only SPICE models will be effective until the new IBIS techniques are
available.
Single line required - cross talk from non SCSI sources not considered
in the model, SCSI line cross talk is not significant within the
transceiver. Therefore multiline models are not required for
transceivers.

The following people agreed to attempt to make their transceiver models
available:

Action item: Dan Smith to provide Seagate transceiver models to the web
site.
Action item: Tariq to provide Adaptec transceiver models to the web
site.
Action item: Larry Barnes to provide LSI transceiver models to the web
site.

11.2 Bus segment termination: owner, Paul Aloisi / Don Getty

No new content information.

Interface is at package pins
Model types: Spice, IBIS details TBD
Terminator type: multimode
Single line only

The following people agreed to attempt to make their terminator models
available:

Action item: Paul A. to provide web site info for the TI terminator
models.

11.3 Transceiver board: owners, Tariq Abou-Jeyab and Matt Schumacher

No new content information.

Interface is at transceiver board connectors, transceiver chip pins, terminator chip pins
Model types: Spice
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

Further detail was provided by Matt in this area as transcribed below:

Listed are some key datapoints to consider for HSPICE simulation of a simple LVD SCSI PCB. Initial simulations will be used to optimize PCB routing topologies. Simulating worst case scenarios will be discussed in a later document, as it will require SPICE model correlation, process corners, multiline SPICE models for cross talk etc.

Request SPICE models:

        check for a driver and a receiver model
        Ask for single line models and multiline models of connectors. Multiline models may take much longer to arrive if you can get them at all. If single line models are used, signal integrity investigation will not include crosstalk.
        Are models for unmated connectors necessary?
        Required models must work for various edge rates (slow, typ, fast)
        Keep the models in a centralized/secure location. Vendors usually distribute them under NDA.
        Some correlation of the models is recommended (compare simulation and lab data)
        Request models well in advance of need

Obtain transmission line geometries from PCB data / design requirements

        These parameters are required: trace width, copper weight of trace and planes, dielectric constants, dielectric spacing within the differential pair, dielectric spacing to the planes and trace lengths of the nets to be simulated.

Generate RLGC matrices for transmission line segments(cline):

        Using a field solver, obtain the RLGC matrices for the transmission line geometries.
        Compare the field solver impedance with the TDR measurement of the coupon.
        Note: the coupon will provide a controlled environment with minimal discontinuities for accurate trace characterization.

Draft a trace topology from the known trace segments and components:

        Draft the transmission line topology
        the drawing below is an example of a simple transceiver board in host bus adapter

Build a spice netlist for the trace topology:

        Do not forget the process variations.

Simulate and review data:

Time domain simulation is sufficient for optimizing topologies.

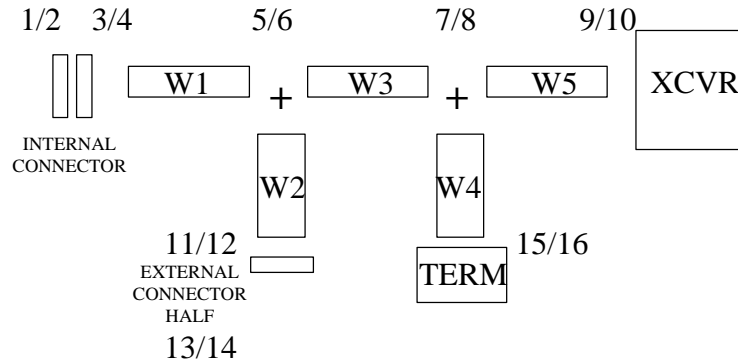W's are SPICE element numbers. All other numbers are node locations.

Figure 2 - Architecture of a transceiver board model (no unused connectors)

11.4 Mated connectors: owner, Martin Ogbuokiri

No new content information.

Interface is at transceiver board and the cable assembly transition
region
Model types: Spice
Connector types: VHDCI, SCA-2, HD68
Mounting style: thru hole, SMT,
single line, multiline

A source for connector models is in place at Molex and the information
guiding to this site will be given to J. Lohmeyer.

Action item: Martin to provide models to the web site for SCA-2, HD68,
and VHDCI

11.5 Cable assembly transition region: owners, Bob Gannon, Greg
Vaupotic

Interfaces are at the connector termination and the uniform media
Model types: Spice same as connector
Construction types: twisted flat, round fanout, laminated round, IDC flat?
Single line multiline

Although there was no new specific content for this matrix element it was noted that the parameter extraction methods described by Dima in his presentation may be excellent for extracting RGC for the cable transition region.

Action item: Rollie O'Groske to provide a plan to get a model for the transition regions.

11.6 Uniform cable media: owner, Jie Fan

Interfaces are at the beginning of the cable assembly transition region on either end.
Model types: Spice
Cable types: flat, round shielded, round unshielded twisted flat?
Single line, multiline

Action item: Jie to provide a cable media model to the web site.

11.7 Backplane: owner, Larry Barnes

Interfaces: connectors mounted on the backplane, directly mounted components,
Model types: SPICE
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

Action item: Larry Barnes to supply component definition and a graphical representation for the backplane (should not contradict the transceiver board if possible)

12. Simulation integration strategy

Further discussion pending progress on the component level simulation work. This will be addressed at the next meeting.

13. System configurations

Not discussed but reaffirmed as needed for the document

14. Data patterns

Not discussed but reaffirmed as needed for the document

15. Data rate

Not discussed, but reaffirmed as needed for the document

16. Definitions:

A comprehensive set of definitions has been created in the draft document.

SPICE, IBIS, model, validation, cable assembly, transition region, verification, accuracy, HDL, VHDL, ASM, ASCM, Veriloq, PCB, backplane, microstrip, stripline, via, discontinuity, cline, lossy, lossless, uniform, attenuation, gain, differential, planar, skin effect, dielectric constant, dielectric loss, loss tangent, conductivity, resistivity, convergence, phase velocity, group velocity, group delay, phase delay, multiline, single line, SLM, MLM, single ended, balanced, unbalanced, mode, element, RLGC, netlist, admittance, transmittance, coupling(K), matrix, S parameters, scattering matrix, ABCD, Y parameters, two-port parameters, and others to be suggested later.

17. Model database strategy (Wallace)

The revised proposed a specific summary of the present plans for the web based database:

• List of companies with existing models.
• What type of models are they. Connector media, transceiver etc.
• Description / intended use
• Path to the model, is an nda required for the model
• Contact info for model support
• What type of model, SPICE, IBIS, HDL.
• Revision history on site.

18. Tools:

This topic refers to identification and properties of specific modeling tools. It was not discussed at this meeting.

18.1 Document framework (Barnes)

Larry Barnes, editor of the SSM document, reviewed the present state and organization of the document. Following is the result of this discussion cast in the form of a table of contents with owners assigned. The numbering may not be accurate in the list below. Note the addition of Dima to the cable assemblies section.

Section owners are to create basic material and submit to Larry Barnes before the next meeting.

1. SCOPE ((Larry Barnes)
2. REFERENCES(Jonathan Fasig)
2.1 Approved references
2.1.1 References under development
2.2 Resources
2.2.1 Publications
2.2.2 Online bookstores & publishers
2.2.3 Other online resources
2.3 Tools
3. DEFINITIONS, ACRONYMS, SYMBOLS, KEYWORDS, AND CONVENTIONS (group)
3.1 Definitions
3.2 Acronyms
3.3 Symbols and Abbreviations
3.4 Keywords
3.5 Conventions
4. GENERAL
4.1 Overview (Bill Ham)
5. METHODOLOGIES
6. MODELS
6.1 General recommendations (Larry Barnes)
6.1.1 Supporting documentation
6.1.2 Behavioral models
6.1.3 Circuit Models
6.2 Cables
6.2.1 Cable media (bulk cable) (Jie Fan)
6.2.2 Transition region (Bob Gannon, Greg Vaupotic)
6.3 Connectors (Martin O.)
6.3.1 Cable connectors
6.3.2 Non-cable connectors
6.3.2.1 RLC transmission line matrix
6.4 Printed circuit boards (Matt S., Tariq A.)
6.4.1 Traces
6.4.1.1 Microstrip
6.4.1.2 Stripline
6.4.1.3 Broad coupled stripline
6.4.1.4 Offset broad coupled stripline
6.4.2 Discontinuities
6.4.2.1 Vias
6.4.2.2 Pads
6.5 Devices
6.5.1 Terminators (Paul Aloisi / Don Getty)
6.5.2 Transceivers (Dean Wallace)
6.5.3 Packages
7. STANDARD MODEL CONSTRUCTIONS
7.1 Host bus adapter / target board (Tariq / Matt S.)
7.2 Point to point / multidrop (TBD)
7.3 Cable assemblies (Dima Smolyansky)
7.4 Backplane (Larry Barnes)
7.5 System model (TBD)
8. MEASUREMENT AND VALIDATION
8.1 Access to measurement points
8.2 Physical measurement points (Greg Vaupotic)
8.3 Behavioral
8.4 Circuit
9. SIMULATION INTEGRATION STRATEGY (Dean Wallace)
9.1 System configurations

9.2 Data patterns
9.3 Data rates

19. New business

No new business was conducted.

20. Next meetings

Scheduled meetings:
Feb 08, 2000 Huntington Beach, CA (Qlogic) 9AM to 5PM
Mar 01, 2000 Manchester,NH (Hitachi) 9AM to 5PM

Future requested meetings:
April 12, 2000 Monterey, CA (Adaptec) 9AM to 5PM

21. Action Items:

21.1 Action items from previous meetings

Status as of the October 28, 1999 meeting is shown.

Martin O. to supply an RGL transmission line matrix (circuit type of
specification) for VHDCI, SCA-2,and HD68 connectors.
Status: done except for HD68

Larry Barnes to do an overview presentation of the IBIS transceiver
model specification.
Status: carried over - handouts provided but presentation still needed

Ham to post the draft minutes of the October 01 meeting after review by
Dean
Status: done

Larry Barnes to propose a multilevel output capability for IBIS to allow
for ISI compensation.
Status: done for multilevel, ongoing for ISI compensation

Jonathan Fasig to draft a proposal for model requirements for passive
interconnects.
Status: done

All matrix element (document section) owners to provide draft input for
the respective sections to Larry Barnes by November 19, 1999. (Provide
input in Word 6/7 format) send to larry.barnes@lsil.com
Status: input received from Jonathan F and Don Getty – others have not
yet responded - action item carried over to next meeting.

Dean Wallace to contact Bob Gannon to determine how he wishes to proceed with the cable assembly transition region.
Status: Done by Ham - Bob will continue in this role (along with Greg V.)

21.2 New action items from present meeting

Larry Barnes to contact John Lohmeyer to expedite the creation of the SCSI modeling web site.
Status: new

Ham to post the draft minutes of the December 01 meeting after review by Dean and the approved minutes of the October meeting.
Status: new

Action item: Dan Smith to provide Seagate transceiver models to the web site.
Status: new

Action item: Tariq to provide Adaptec transceiver models to the web site.
Status: new

Action item: Larry Barnes to provide LSI transceiver models to the web site.
Status: new

Action item: Paul A. to provide web site info for the TI terminator models.
Status: new

Action item: Rollie O'Groske to provide a plan to get a model for the transition regions.
Status: new

22. Adjourn

The meeting adjourned at 6:00 PM