# 00-103r0   Ultra-320 SCSI Implementing 1.8x Transmit Pre-compensation

Richard Uber

Quantum Corporation

- Amplitude sensitivity to common-mode voltage.
- Effects on driver Z_{out} and common-mode operating point.
- Feasibility of driving output stages harder.
- Feasibility of larger output stages.
- Slew rate issues.
- Effects on NEXT and FEXT.
- Power dissipation concerns.
- Power efficiency of a boost driver strategy.

- Can we drive more current with existing current-mode drivers?
- Simulation circuit for observing differential V_{swing} and I_{cm}
  - Without terminator, negation swings smaller by 115mV
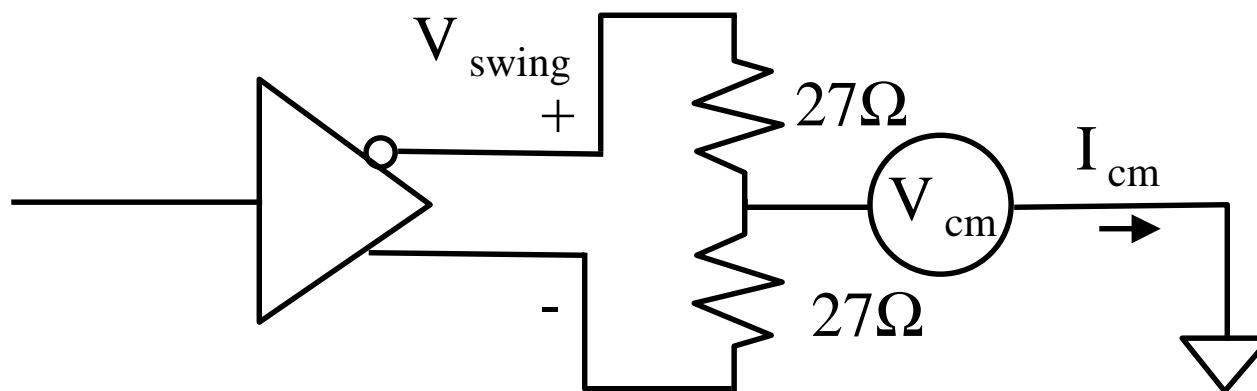
- LVD V_{swing} for V_{cm} swept from 0v to 3.0V
- Currents are highly variable outside of the allowed common-mode range.

Increased driver amplitude
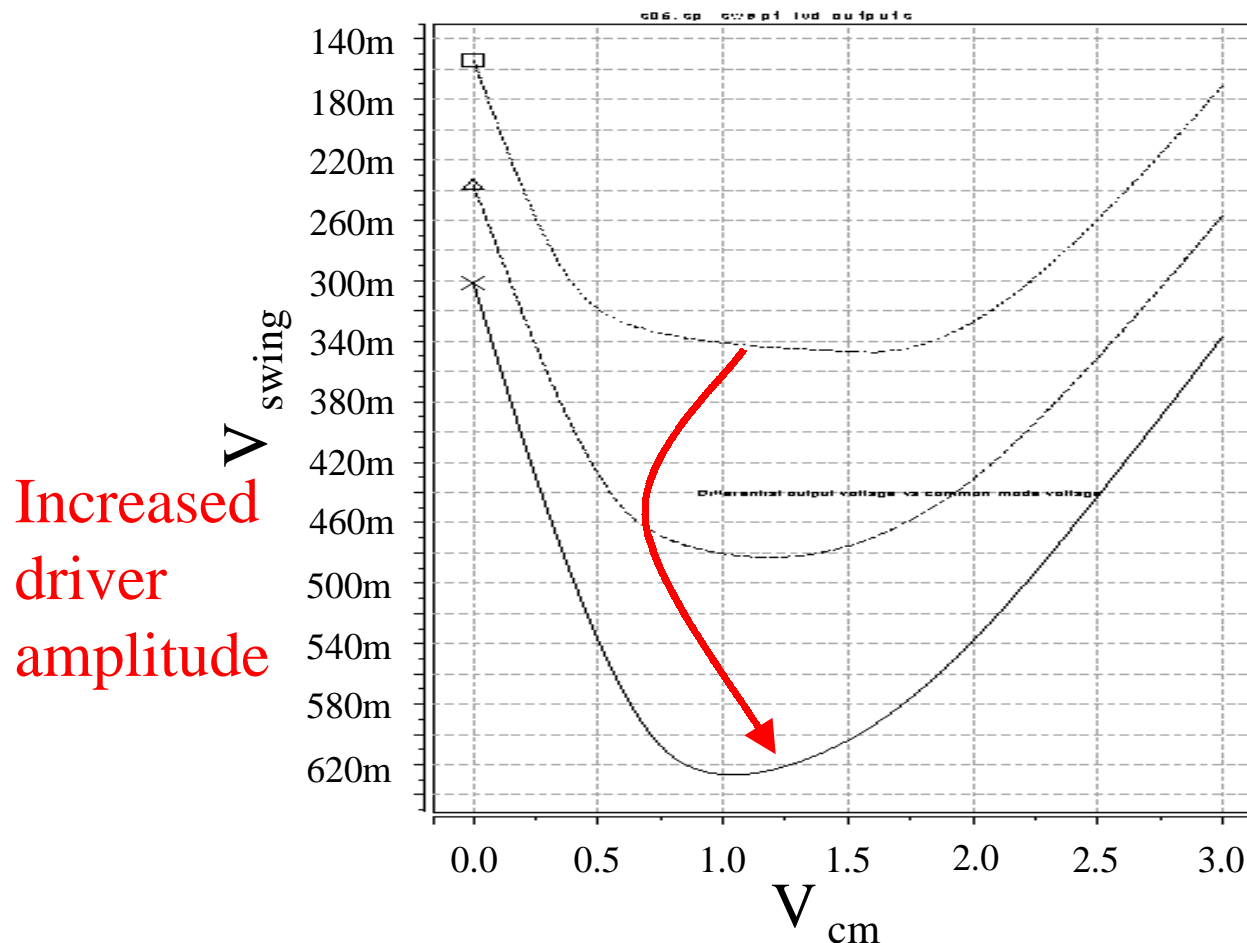
- LVD I $_{cm}$ for V $_{cm}$ swept from 0v to 3.0V
- Currents are highly variable outside of the allowed common-mode range
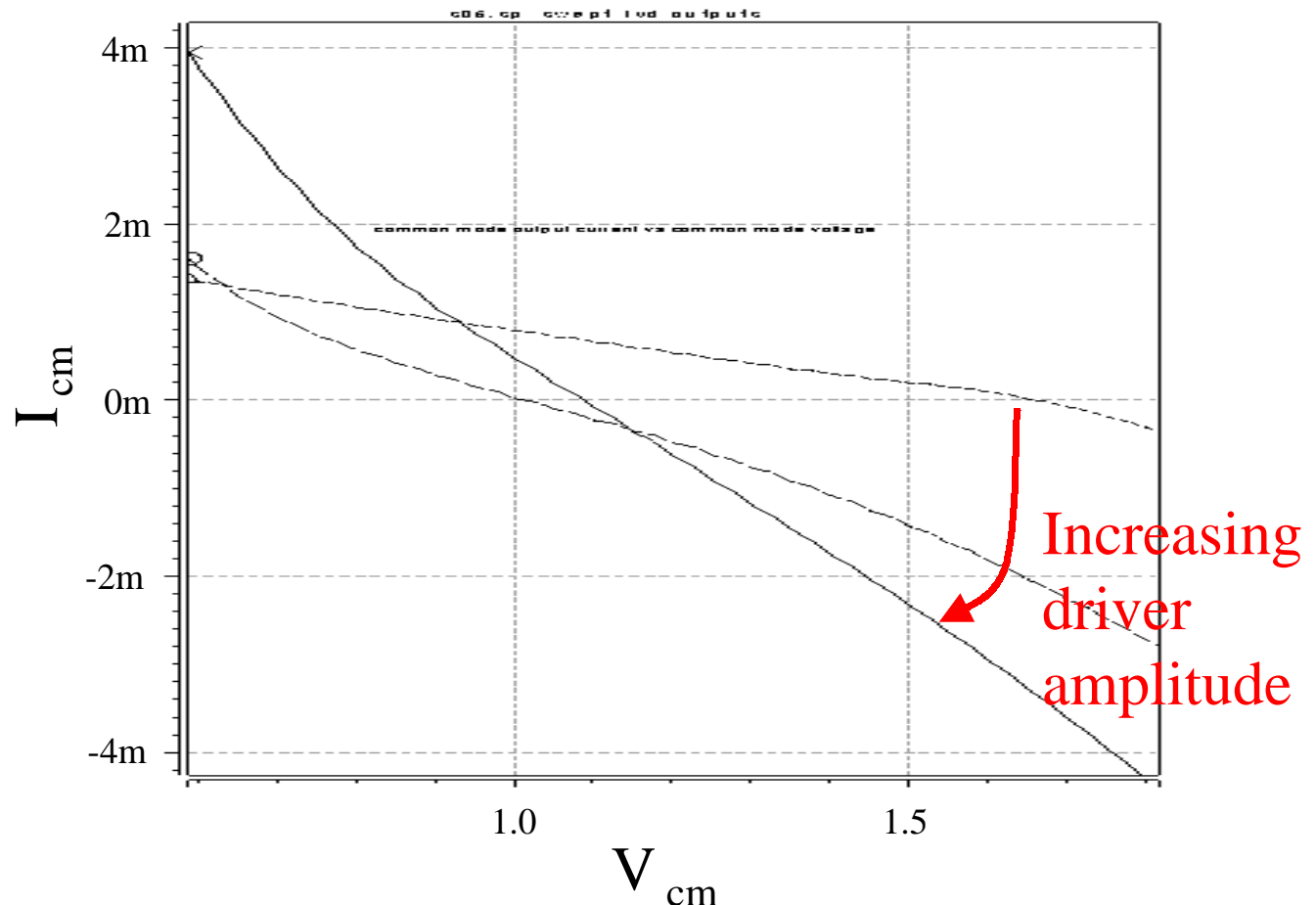
Increasing driver amplitude
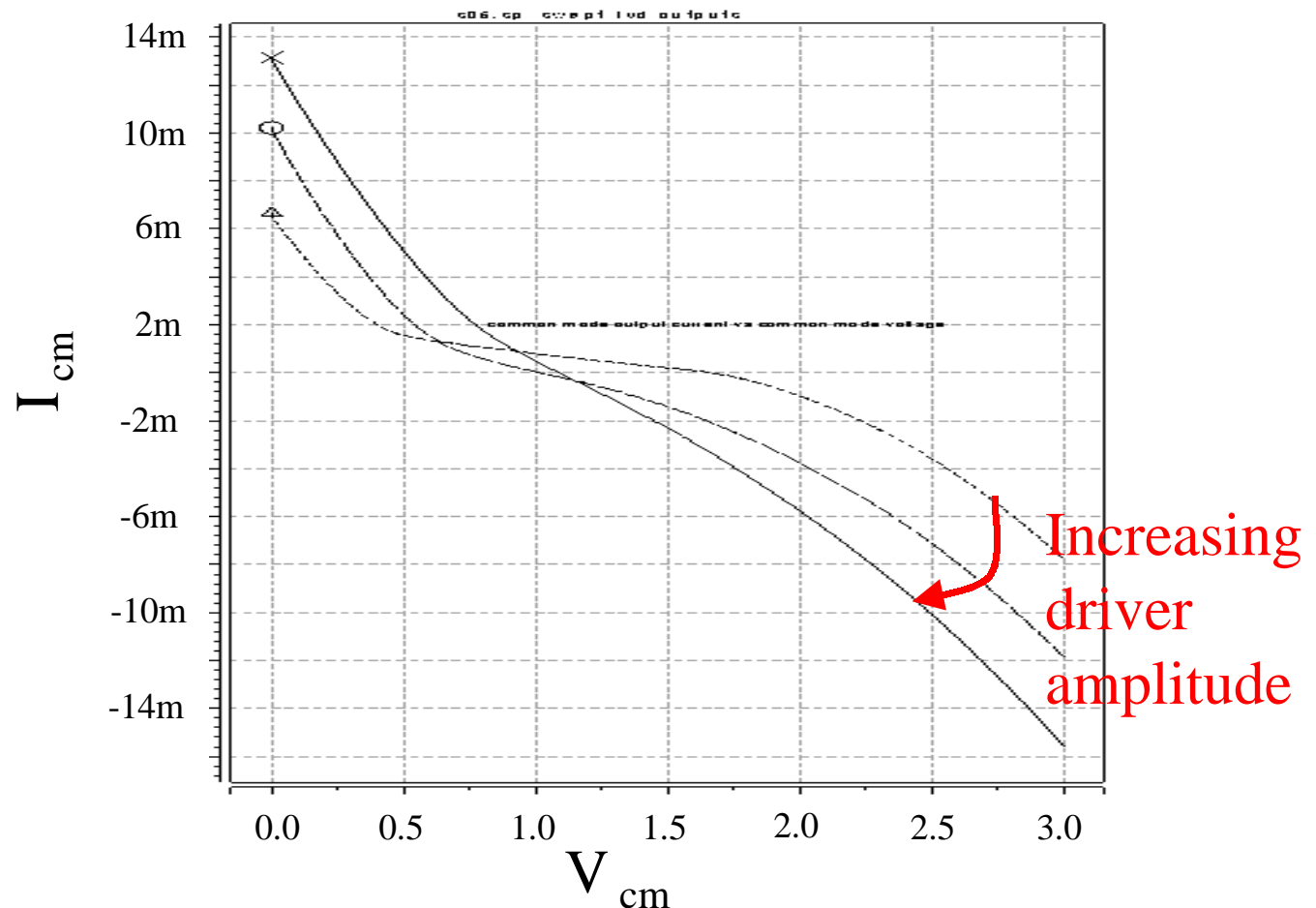
- Usable range (0.855V - 1.645V) V_{swing} versus V_{cm}
- Linearity degrades with increasing signal amplitude

Increasing driver amplitude $\Rightarrow$ increases non-linearity

pk-to-pk non-linearity
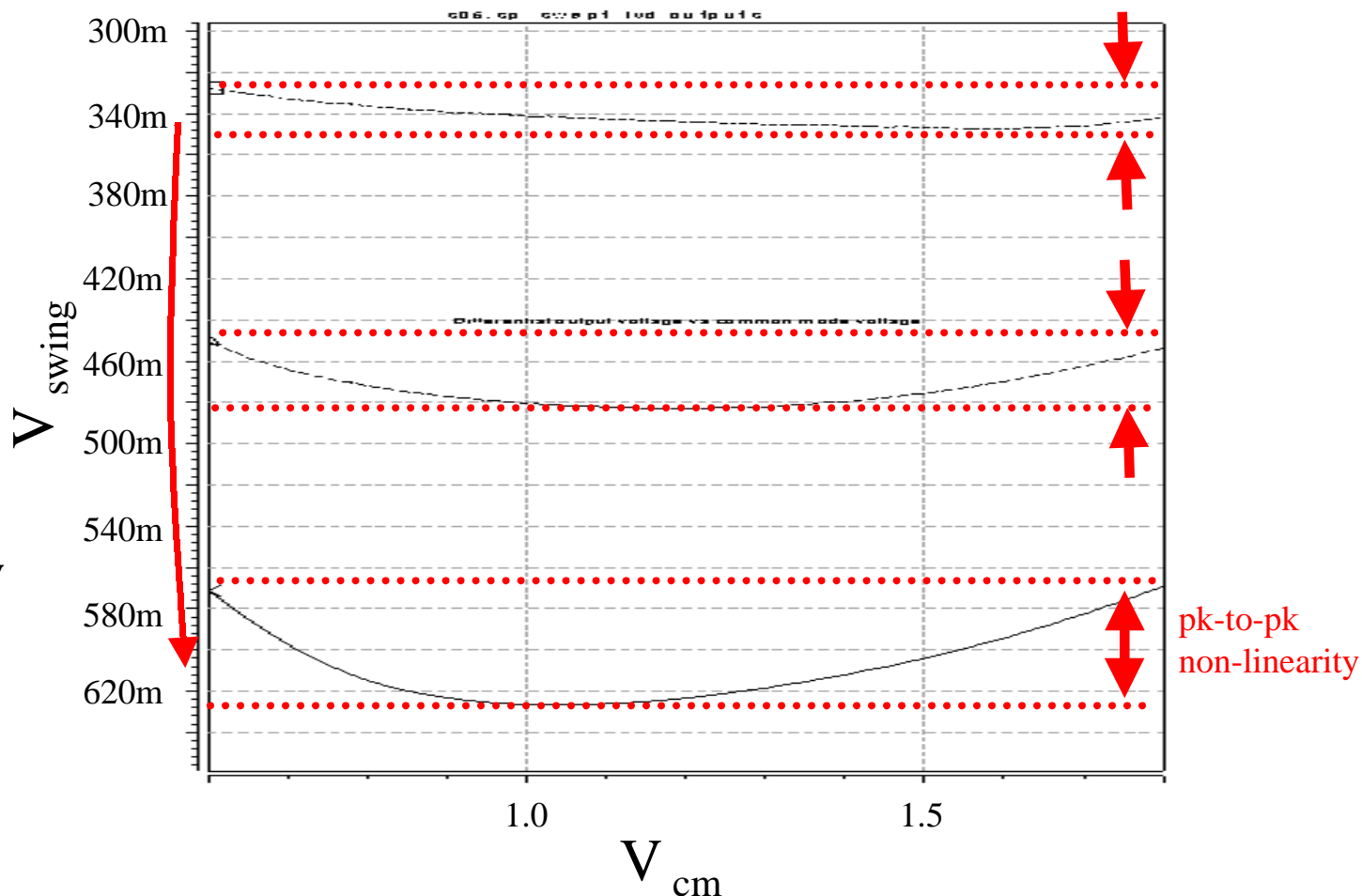
- Usable range (0.855V - 1.645V) I_{cm} versus V_{cm}
- Linearity degrades with increasing signal amplitude

- Differential V_{swing} becomes a strong function of V_{cm}.
- D.C. common-mode current increases (lower Z_{out} for LVD current mode driver).
- Current sources are less ideal.
- Common-mode noise from 3.3V supply increases.
- Turning on and off a "boost driver" will result in common-mode glitches during driver enable and disable.
- Turning on and off a "boost driver" will result in a high frequency common-mode pulses on the bus.

- Consider a 11001100 data pattern, on a driver with 1.0mA of common-mode mismatch.

- An 80Mhz common-mode signal will be present on the bus, with levels 1.0mA and 1.8mA.

- Common-mode voltage waveform depends on the local common-mode line impedance and on common-mode reflections off of the terminator.

110011001100
differential waveform
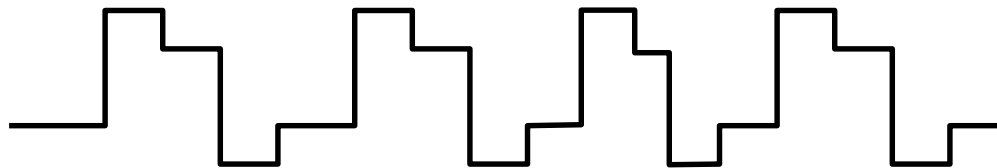
110011001100
Common mode waveform

- A 68 wire cable can have up to 32 wires with identical common mode waveforms.
- Common-mode cross-talk is not helped by twisting wires.
- EM Radiation may become a concern.
- At 80MHz a 2 meter cable is an efficient antenna.
- Question: Can we allow more common-mode content on the bus?

- Die area increases
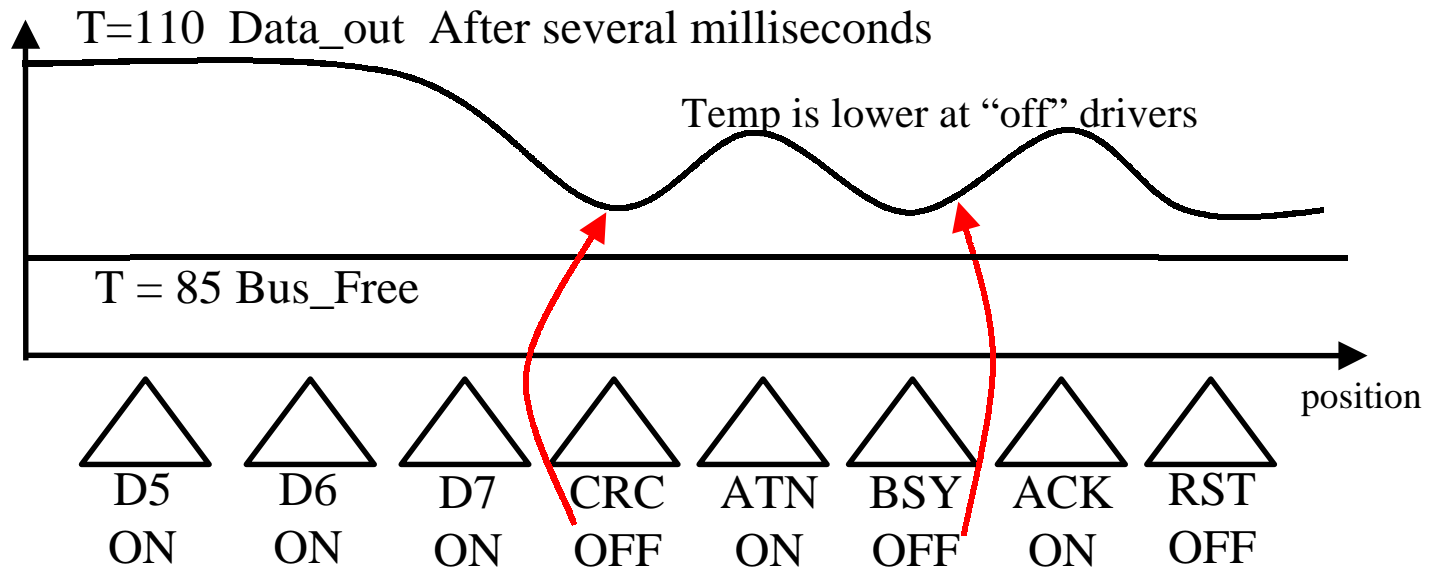- SCSI pads already a large fraction of ASIC die area
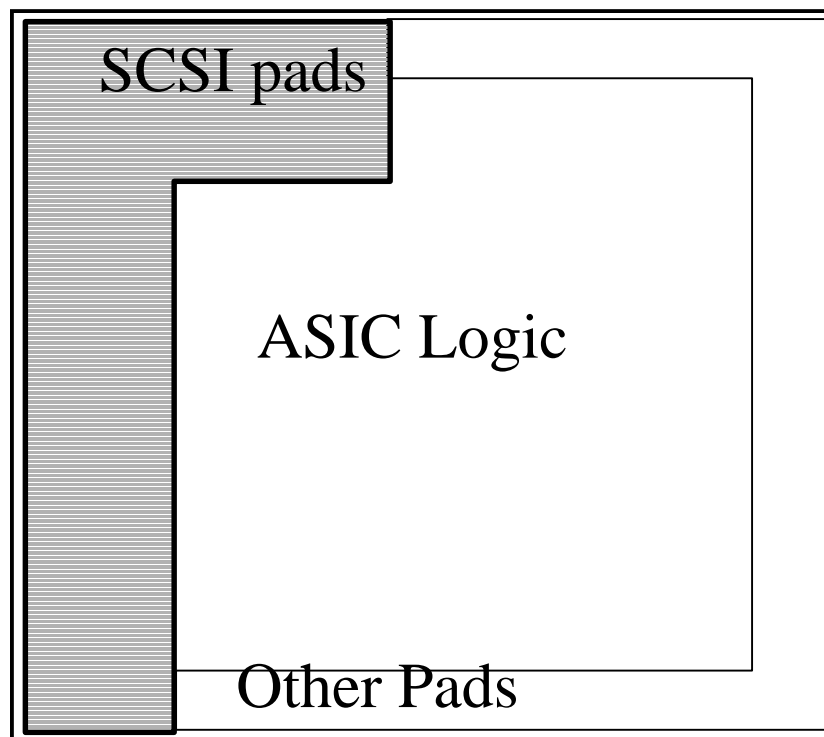
- Capacitance would increase for an "off" driver
  - Estimate an increase of 1.2 to 2.5pF to ground on bus- and bus+.
  - Possible problem with 15pF limit in standard for some vendors.
  - Very likely problem with the tighter capacitance limits in some customer purchase specs for most vendors.
  - Backward compatibility problem (Fast-40 or Fast-80) for back-planes which were marginal with current generation drives.
  - More capacitance would invalidate all eye-diagram data taken to date.

- Some back-plane impedance would drop below 85 Ω with added capacitance.

- Need feedback from SCSI bus integrators on acceptability of higher LVD capacitance.

- Chip heating will be greater as average drive is increased.
- Power delivered to bus increases by the product of the boost factor (1.5, 1.8, …) and the transition density (100% for a 101010 pattern).
- Larger thermal gradients across die, making line to line timing de-skew less accurate.
- Larger delta temperature between first bits in data transfer and those driven after thermal equilibrium is reached.
- In SCSI targets, LVD power already over half of die power.
- More elaborate thermal management on target PCBs?
- Added power in the pad ring will undermine the chip's timing performance.

- When LVD drivers are enabled on the bus, it takes over a millisecond to reach thermal equilibrium.

- Driver temperature also depends on adjacent heat sources (other enabled drivers).

- The temperature difference between REQ/ACK and Data will change over time.

Thermal profile of driver output stages parallel to die edge

T=110 Data_out After several milliseconds

Temp is lower at "off" drivers

T = 85 Bus_Free

position

| D5	D6	D7	CRC	ATN	BSY	ACK	RST
ON	ON	ON	OFF	ON	OFF	ON	OFF

- CAD tools cannot cope with elements at different temperatures.
- Adding more heat to the pad ring makes timing optimization harder.

Driver j

Edge of die

Driver i

Elements match
Clock wire lengths match
Q wire lengths match
Flip-Flop temperatures different

… chip core

Temperature perpendicular to die edge

Drivers Enabled

T = 85 Bus_Free
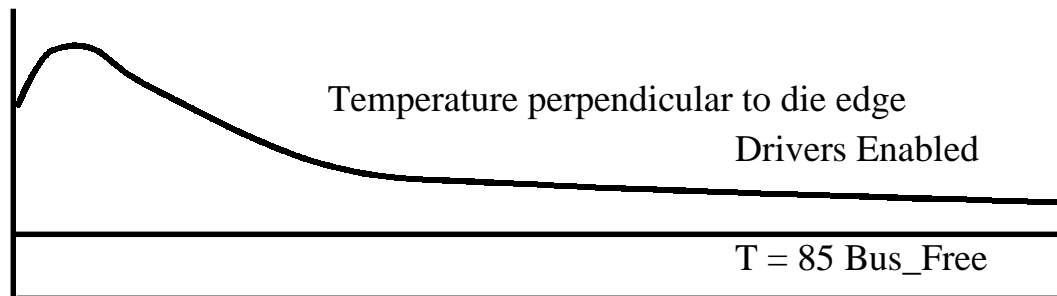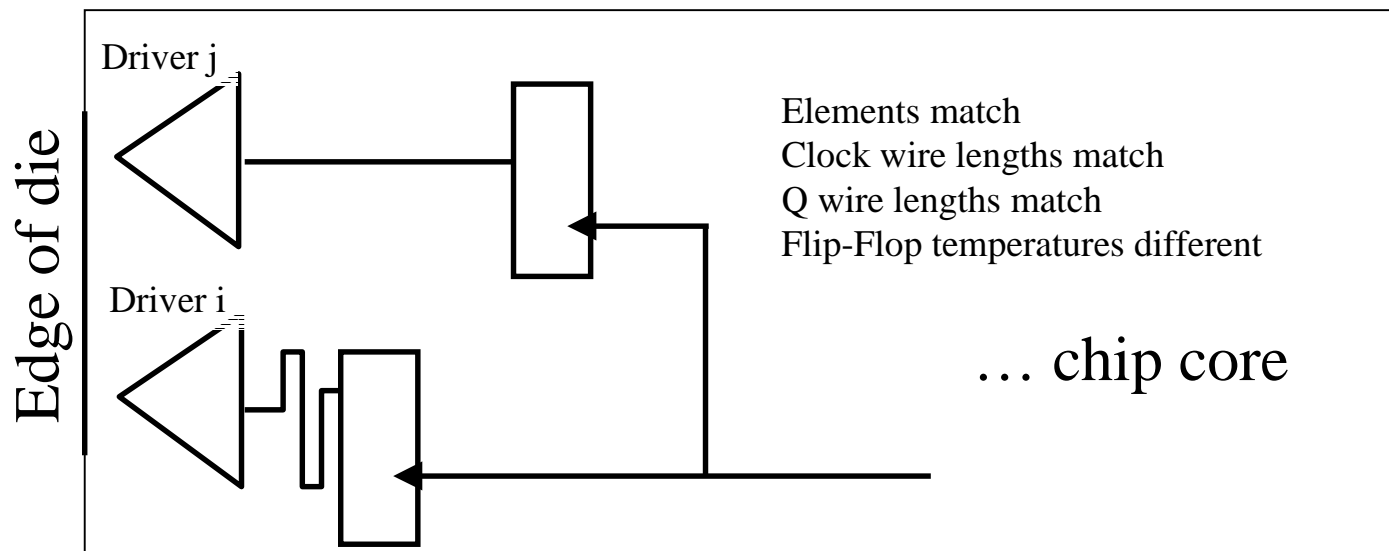
- The higher swings must be obtained with the same rise and fall times as in U160 products.

- Higher slew rates result, and will result in increased ringing at the transmitter.

- Higher slew rates will increase the number of stubs which cause problem reflections.

- Currently, any misalignment of pull-up and pull-down pre-drivers leads to a common-mode glitch during a data transition. With a "boost driver", there are 4 pre-drivers to align instead of the current 2 pre-drivers.

- Sensitivity of common mode transition noise to the ASIC chip package and board mismatches (between bus+ and bus-) will increase.

- Near End Cross-Talk (NEXT) will increase due to the greater $\partial I / \partial t$ on the driven wire pairs.

- Far End Cross-Talk (FEXT) will increase due to the larger voltage swings being driven.

- Ratio of coupled cross talk signal to quiescent signal will increase by the boost ratio (1.5, 1.8, …).

- Increased intra-chip coupling through power and ground rails from non-constant current driver.

- Worst case buses have substantial series resistance.
- Net load R is 58 Ω.
- Adding 1.0mA to driver, adds 58mV to driver (cross-talk source)
- Adding 1.0mA to driver adds only 41mV at far terminator.
- Adding energy at the transmitter is inefficient.

Terminator   R $_{cable}$ R $_{back\text{-}plane}$ Terminator

100Ω 4Ω 16Ω 100Ω

driver   4Ω 16Ω
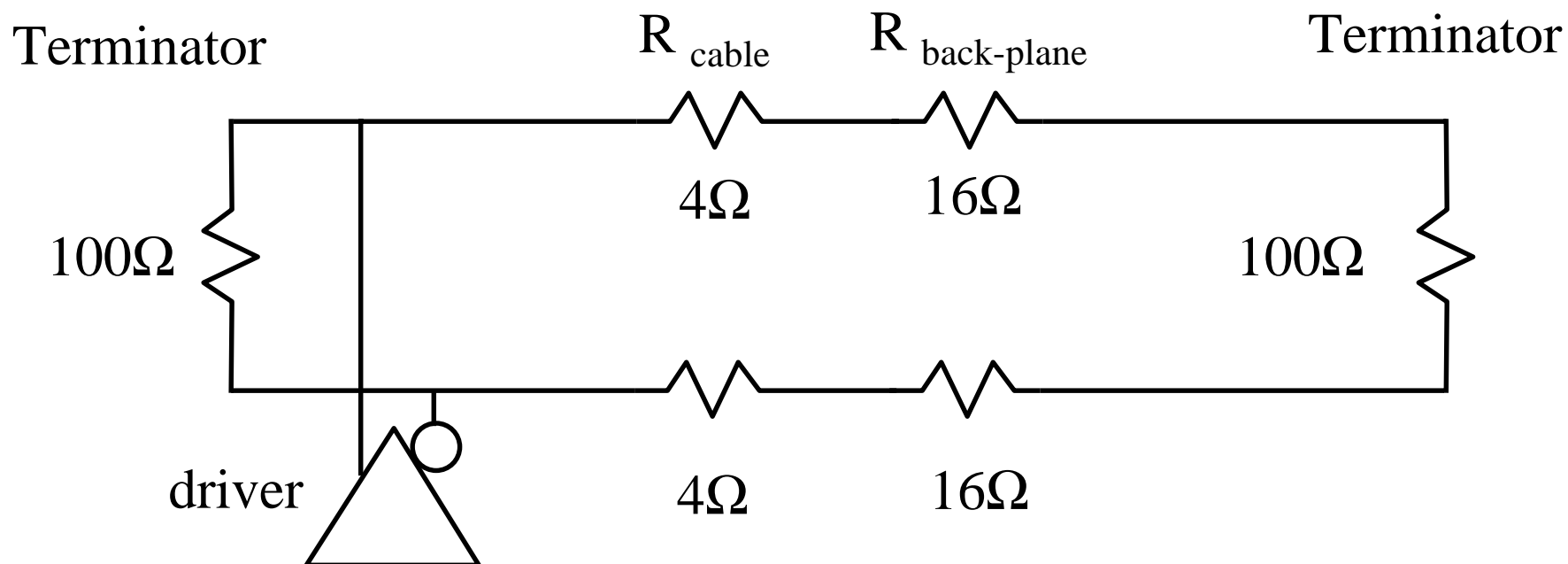
- "Boost only on transitions" is under consideration.
- Must tightly align edges on main driver and boost drivers.
- Slew rate increases to maintain rise/fall times
- Cross-talk increases
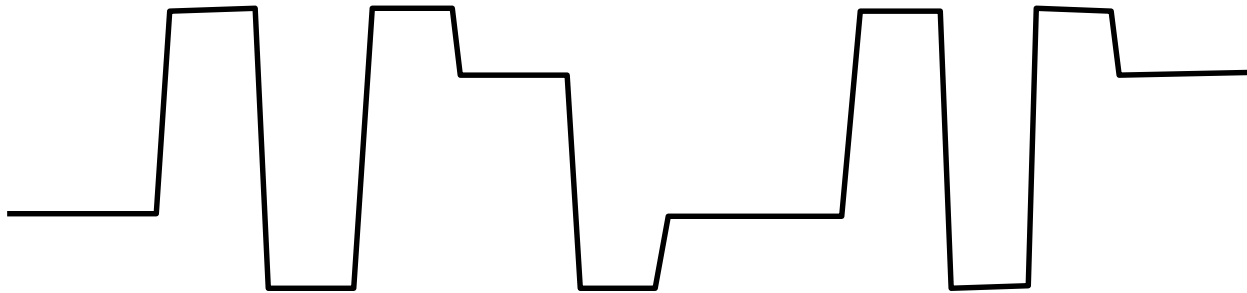
- "Decrement after count = N" is under consideration
- Secondary edge can be slower, reducing cross-talk.
- Slower edge harder to control for common mode transient.
- Edge type 1:(+/-nom level) $\Rightarrow$(-/+nom level) transition
- Edge type 2:(+/-reduced level) $\Rightarrow$(-/+nom level) transition
- Edge type 3:(+/-nom level) $\Rightarrow$(+/-reduced level)
- Timing de-skew can only adjust one class of transition edge.

Edge types: 1   2   3   2   1
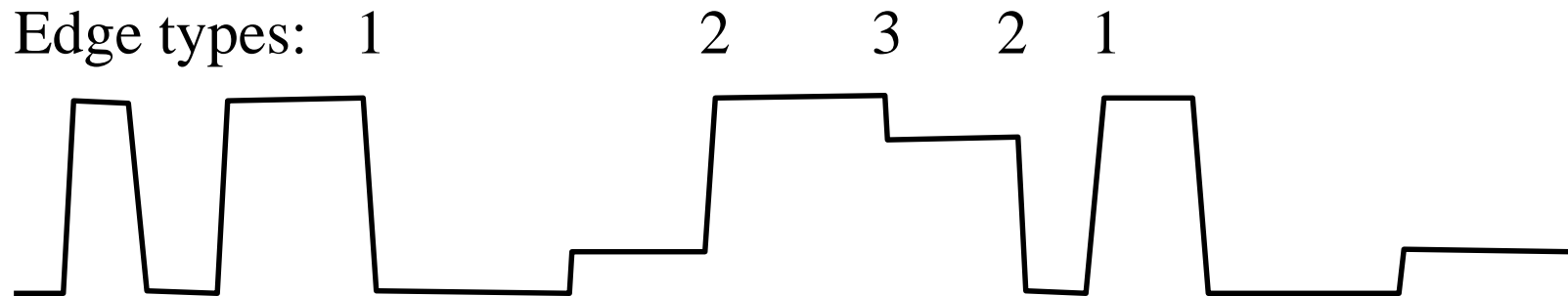
❶ Current source non-linearity versus drive current tradeoffs.

❷ Quantify added common mode signals and noise.

❸ Quantify EM radiation issues and limits for cables with substantial in-phase common mode signals.

❹ Quantify additional capacitance needed.

❺ Quantify power increases, and resultant local junction temperatures.

❻ Include temperature profile issues in timing budget.

❼ Study optimal transmitter pre-comp drive levels.

❽ Study possible transmitter pre-comp algorithms.

❾ Investigate alternatives to transmitter pre-comp.

Quantum™

1. How much more pin capacitance is acceptable for U-320 capable devices with respect to signal integrity?

2. How much more pin capacitance is acceptable for U-320 capable devices with respect to backward compatibility?

3. How much additional common mode content is acceptable on U-320 drivers?

4. What is the amplitude threshold at which an 80Mhz common mode signal become an FCC problem?

5. Consensus is needed on cross-talk measurements and limits.

6. Can transmitter pre-comp be left vendor specific, or can cross-talk interfere with signals driven by the receiver device?

❶ A transmitter pre-comp which helps ISI without causing new problems is not trivial.

❷ The high multipliers (1.5 - 1.8) are a major departure from existing LVD technology, and add a lot of risk to U-320.

❸ There is a high likelihood that side effects of high ratio transmitter pre-comp will cause problems with backward compatibility and multi-vendor interoperability.

❹ We should consider other alternatives.